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SENSING CIRCUITS FOR MULTIWIRE PROPORTIONAL CHAMBERS

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16. Abstract <p>The objective of this study program was to develop a realistic plan for the fabrication of sensing circuits for Multiwire Proportional Chambers. In this report the detailed design of the proposed circuits is described and the results of computer simulations are presented. The fabrication processes for the CMOS on sapphire sensing circuits and hybrid substrates are outlined. Several design options are described and the cost implications of each discussed. In the concluding chapter the results of the study program are summarized and recommendations for the prototype phase are made.</p>			
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PREFACE

The objective of this study was to develop a design approach for the fabrication of sensing circuits for Multiwire Proportional Chambers. The scope of study included justification of the technology selection, design of certain circuit elements to establish the approach feasibility, use of computer simulations and other analytic methods for predicting circuit performance, and a trade-off study to determine which of several design options is most cost effective. In this study it was shown that the Multiwire Proportional Chamber Sensing Circuits can be built using CMOS on sapphire and that these circuits should approach the performance goals originally contained in the RFQ. It should be noted that the high speed and low power capabilities of the CMOS on sapphire technology make it clearly superior to any other established technology for this application. It is therefore recommended that the sensing circuits be fabricated using CMOS on sapphire technology. To be most cost effective each chip should handle not more than 32 inputs and each chip should be mounted on its own hybrid substrate. Direct attachment of the sensing wires to the hybrid substrate should be used if it does not interfere with the wire wrapping.

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1. INTRODUCTION

1.1 Purpose

The purpose of this study was to define a program for the development of Readout Integrated Circuits for Multiwire Proportional Chambers. Multiwire Proportional Chambers are used to determine the direction and fluence of ionizing radiation passing through the chamber. Each layer of the chamber is made up of an array of equally spaced parallel anode wires in a plane equidistant from two planar conductive cathodes. Typical spacing between the cathodes is 8 to 15 millimeters. The top cathode for one plane of anode wires can also serve as the bottom cathode for a plane of anode wires strung perpendicular to the lower wires. By repeatedly stacking anode wires and cathode planes, a three dimensional array can be achieved. When an ionizing particle passes through the chamber it ionizes the enclosed gas. The positive ions are collected on the cathode. The electrons drift toward the anode wire and are accelerated by the high electric field surrounding the wires, causing charge multiplication. The sum of the primary plus secondary negative charges are collected on the anode wire where they are to be sensed by the integrated circuits. From this information a three dimensional track pattern can be established. The purpose of the present study is therefore to develop a program for integrating multiple sensing circuits on a single chip and mounting this chip in a manner that a simple interface to sensing wires can be achieved.

1.2 Scope

The present study is limited to the design, fabrication and packaging of the integrated sensing circuits. The installation of the proposed hybrid package into the MWPC is not covered directly although two possible hybrid approaches are described and the metallurgical requirements of each are discussed.

Under this study two CMOS on Sapphire sensing circuits were extensively simulated. The justification for using CMOS on Sapphire technology, namely high speed and low power, is discussed in Chapter 2. Data from the sensing circuits will be loaded in parallel into a static shift register and read out serially at 10 Mhz. The shift register has been designed and simulated. A preliminary layout of the repetitive portions of the integrated circuit was performed to determine the number of bits which could be reasonably incorporated on a single chip subject to size restraints imposed by yield and cost factors.

Two hybrid approaches are described. The selection of one approach has been left to the NASA technical officer based on the ease and reliability with which his other contractors can assemble the hybrid into the MWPC.

A cost analysis has been performed to show the impact of the various technical options on the cost parts, both in the prototype and in the production phases.

2. DESIGN OBJECTIVES

This section details the design objectives of the circuit that is to interface with the MWPC. This circuit will be capable of digitizing an input signal as a logic "1" or logic "0". The digitized output will then be loaded in parallel into a parallel/serial shift register. The shift register will output the data serially. The following describes the desired performance characteristics of the MWPC circuit:

2.1 Input Signal Characteristics

The signal into the circuit is charged from one of several sense wires of a multiwire proportional chamber. The primary charge collection at the sense wire or anode occurs in approximately 100 nanoseconds. A secondary rise in the charge collected at the anode occurs after the first 100 nanoseconds as shown in figure 2-1. The minimum signal amplitude will be $\sim .1$ picocoulomb. The anode or source capacitance that will collect the charge will vary from 1 to 5 pf depending on the MWPC design. Variation of the capacitance from line to line will be $\pm 10\%$.

2.2 Circuit Performance Characteristics

1. 32 to 64 parallel inputs with signal characteristics as specified above.
2. Each signal input must contain a sample gate, with all gates controlled by a common signal.
3. In the gate open (non-sampled) condition, input resistance is to be fixed such that the charge signal decay time constant is approximately one microsecond. This is required to clear unwanted charge from input capacitance which accumulates independent of "signal" charge.
4. Each sampled analog signal will be digitized according to a reference threshold. The threshold will be applied externally and will be common to all inputs. Threshold range should be approximately 20X. Threshold variation may be no more than $\pm 10\%$ between different devices. Temperature variation of preset threshold may be no more than $\pm 10\%$ over the operating range of -20°C to $+40^{\circ}\text{C}$.
5. Inputs must be protected against transients, of either polarity, with an energy of about 10^{-2} joules. This is to protect the

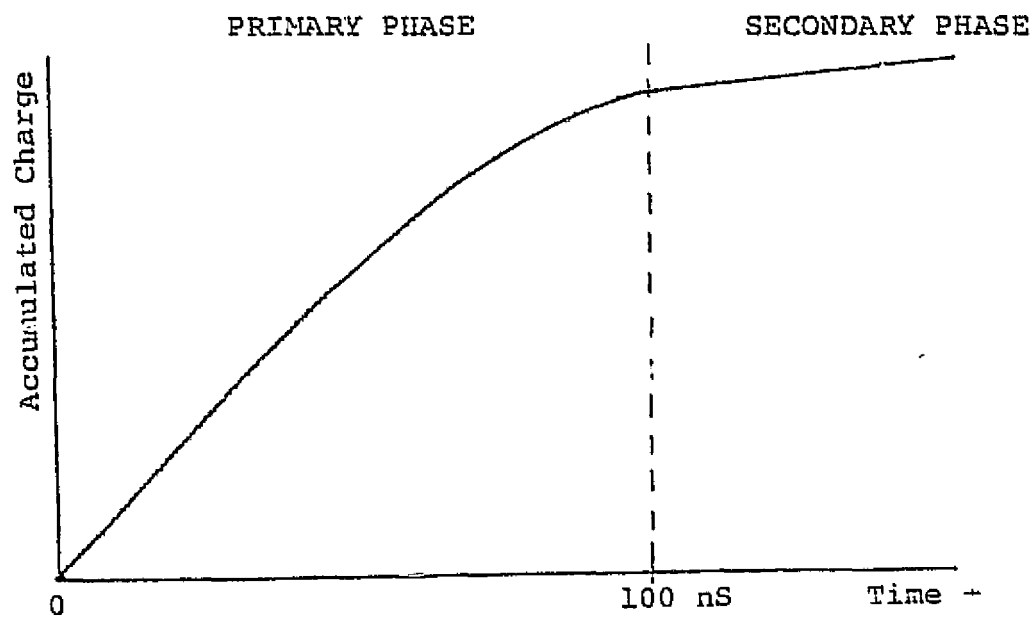


Fig. 2-1. Charge Accumulated on Sense Wire

input against a corona discharge that might occur between the anode wire and the cathode. This discharge is believed to be equivalent to discharging a 1000 - 2000 pf capacitor charged to as much as 5000V through a resistance of less than 100Ω. The energy of this discharge is, therefore, roughly 10⁻²j. In the event an input is destroyed due to a large transient it is essential to have the remainder of the circuit function normally.

6. Device will have serial data input compatible with output to allow concatenation (stringing) of multiple devices. TTL or CMOS output signal levels are desirable.
7. Shift register shall be static or "quasi-static" with storage time of at least 0.1 sec at 40°C. Dynamic (refresh) techniques are not desirable.
8. Clocking to be single or two phase of frequencies up to 10 MHz. TTL or CMOS clock levels are desirable.
9. Quiescent power ≤ 10 microwatts per input. Power at 10 MHz ≤ 100 microwatts per input, including clock power.
10. Package configuration to be such that MWPC sense wires spaced at 0.032" O.C. may be accommodated. It is anticipated that packaging may be a dominant consideration with regard to cost and feasibility of the subject device.

End item cost per parallel input shall be as economical as feasible but not greater than \$4.00 per parallel input.

3. CIRCUIT DESIGN

3.1 Block Diagram

Figure 3-1 is a diagram of the functional elements of the MWPC chip. As seen from the diagram four power supply voltages are required - V_{SS} (ground), V_{DD} (main power), V_{R1} (bias voltage), and V_{R2} (reference voltage for amplifier sensitivity control). Also shown in the diagram are the sense amplifiers and their corresponding shift registers. Input signals are compared against the reference signal by the sense amplifier which outputs a logic "1" or "0" depending on the outcome of the comparison. The sense amplifier is enabled by ϕ_1 . ϕ_2 is used to load the data from the sense amplifier into the shift register. Once loaded, data may be shifted out serially. Notice that a serial data input is provided so that chips can be cascaded.

Three possible versions of the chip were considered - one with 32 bits, another with 48 bits and a third with 64 bits. The 32 bit version would have 41 pads which can easily be handled for wafer testing. The 48 bit and 64 bit chips would have 57 and 73 pads respectively. Testing these on the Tektronix S3260, which is limited to 48 pads, would require multiple passes. Furthermore, it is desirable to be able to package some parts for prototype evaluation in standard packages, preferably in dual-in-line packages. Unfortunately, the largest available dual-in-line packages has only 64 pins.

The only technical advantages in choosing a 48 bit or 64 bit design is that the overhead, i.e. the output buffers, power lines, reference lines, etc. are distributed over a greater number of inputs. This will result in a reduction in the total number of connections and the total power for the MWPC. However, the cost per bit for the 48 bit chip and the 64 bit chip would be significantly greater than for the 32 bit chip as discussed in the Cost Trade-Offs (Section 5.2). In summary, the 32 bit version is preferred because it's pin count is within the maximum number of pins normally encountered on integrated circuits and the price per bit will be less than for the larger chips.

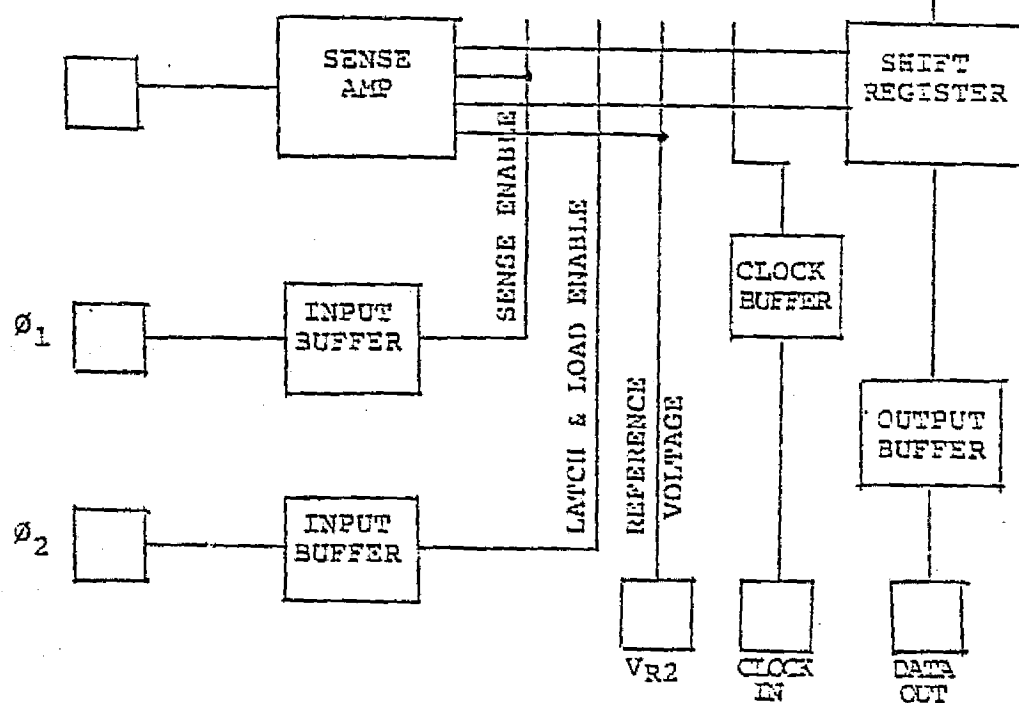
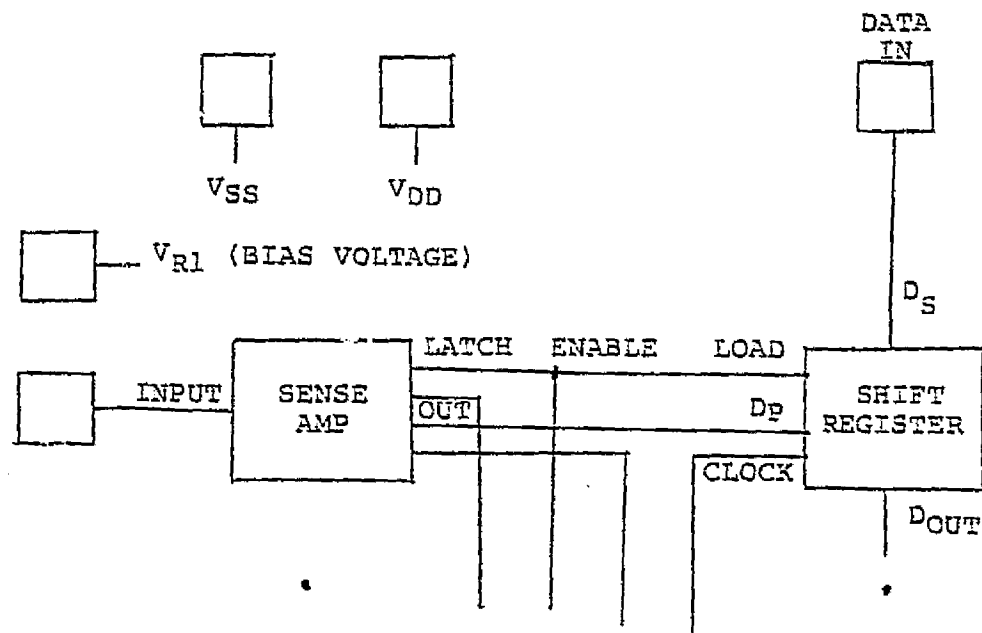


Fig. 3-1
Block Diagram of MWPC Chip

3.2 Sense Amplifier

To understand the development of the sense amplifier circuit it is first necessary to define the type of signal to be detected. The signal is developed by depositing charge over a period of about 100 ns onto a source capacitance, C , of 1 to 5 pf. This causes the voltage on the capacitor to rise by an amount equal to $\Delta Q/C$. After the charge has been deposited a sense command signal will be presented to the sense amplifier. The sense amplifier must then sample the input signal and output a logic 1 or 0 depending on whether or not the total accumulated charge has exceeded a threshold value which must be made adjustable by a factor of 20:1.

The most common way to detect small signals in MOS digital circuits (especially RAMs) is to use a cross coupled transistor pair as a differential pair. Differential amplifiers find widespread use in monolithic technology since this type of circuit is not sensitive to chip to chip parameter variations but rather to parameter matching of adjacent components which is quite good for monolithic circuits. The transistor pair is cross-coupled so that regeneration will take place after the differential signal has been applied. A logic state will thus be developed and maintained.

Figure 3-2 shows a CMOS version of the basic MOS cross coupled amplifier. Transistors Q3 and Q4 form the cross coupled transistor pair used in the initial sensing phase. Transistor Q5 is a power supply switch used to turn off the ground return of the N channel transistors, Q1 and Q2, during the initial phase. After a large differential signal has been developed across Q3 and Q4 through regeneration Q5 is turned on so that a CMOS latch is formed which results in CMOS logic levels appearing at nodes 1 and 2.

To increase the gain of the circuit shown in Figure 3-2 a preamplifier stage was added. Two different preamplifier stages were considered - a common gate configuration and a common source configuration. Because small signals are to be detected both of these stages require a bias current to offset the threshold voltage of the enhancement transistors. Both of these circuits will now be examined in detail.

Figure 3-3 shows the complete circuit diagram of the sense amplifier using a common gate preamplifier. Also shown in the diagram is the circuit used to generate the reference signal and the circuit used to simulate the input signal. The reference signal is developed across a capacitor divider network consisting of C1 and C2 and is controlled by Q10 and

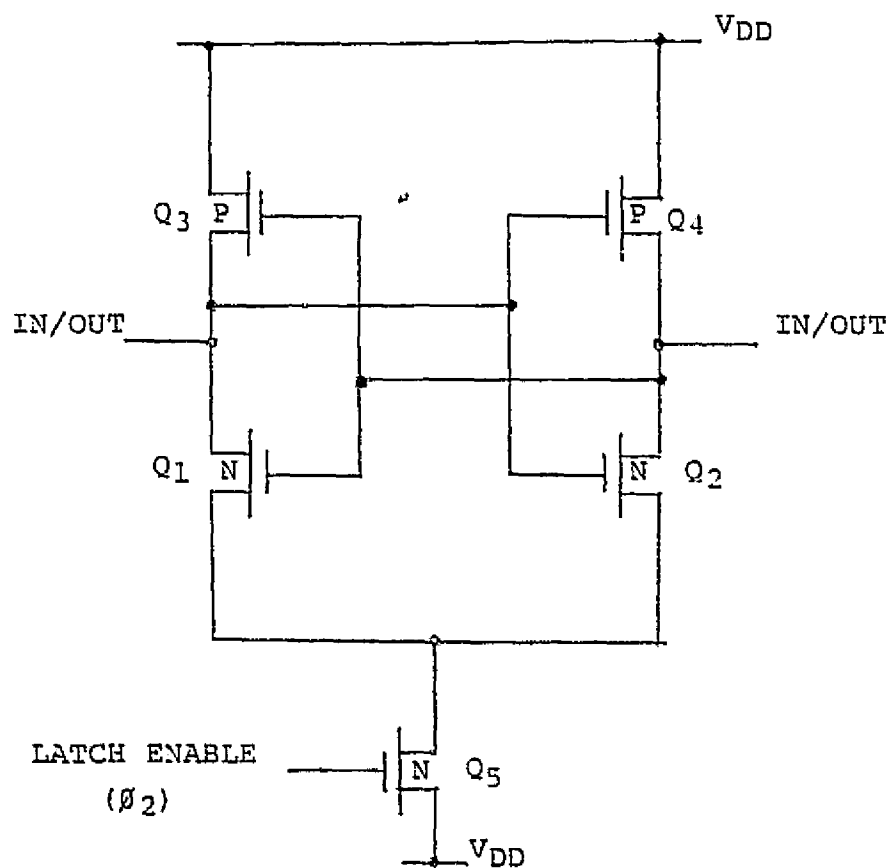
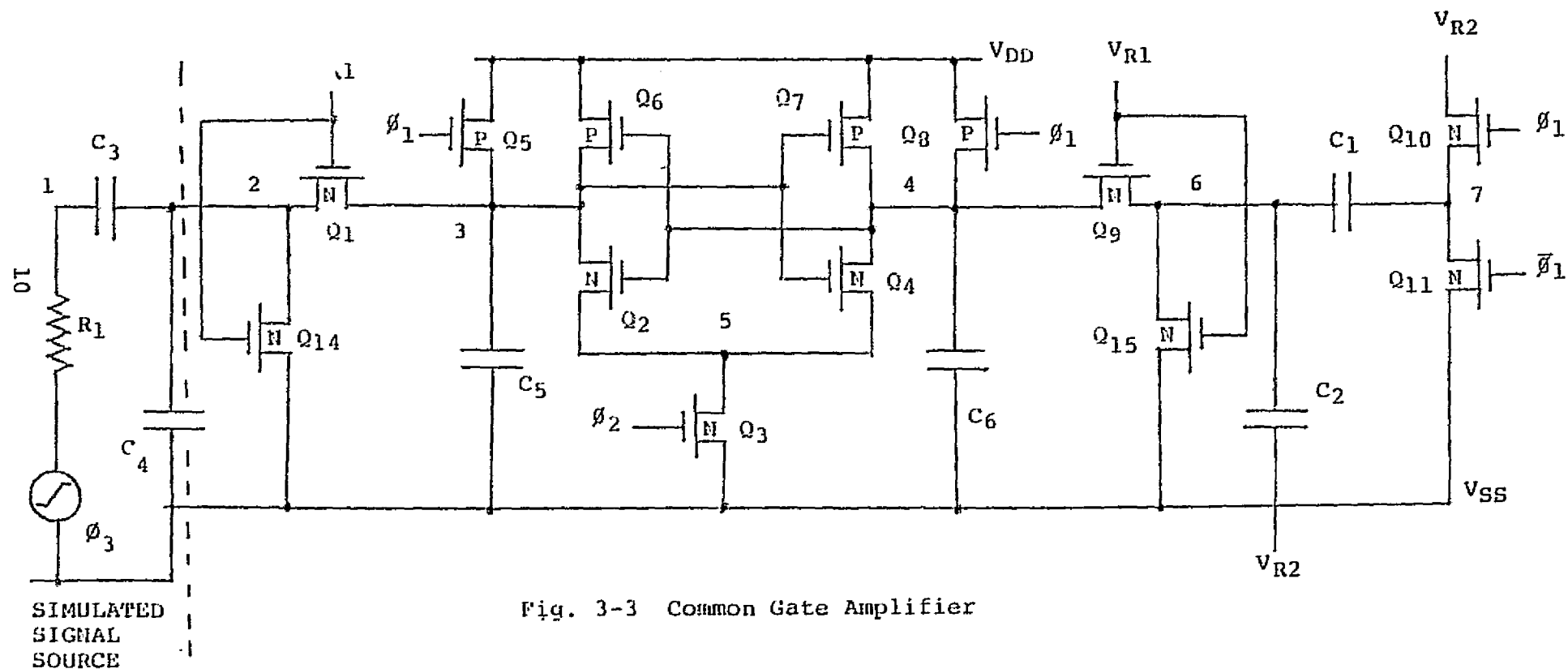


Fig. 3-2. CMOS Cross Coupled Latch



Capacitor Description

- | | | |
|--------------------------------|---|---|
| C ₁ | - | Reference Divider |
| C ₂ | - | Reference Divider |
| C ₃ | - | Coupling Capacitor used in Simulated Source |
| C ₄ | - | Source Capacitance |
| C ₅ &C ₆ | - | Capacitors Used in Simulations to Represent the Loading by the RS Latch |

Q11. The equation for the reference signal amplitude is:

$$\Delta V = - \frac{C_1}{C_1 + C_2} V_{R2} \quad (1)$$

This configuration was selected for reference signal generation since no spurious charge is deposited on the reference node as a result of a switching transient. A negative reference signal was selected so that both capacitors, C1 and C2, remain in strong accumulation throughout the charge transfer cycle. Severe variations in charge transfer would occur if either capacitor operated in the nonlinear region. VR2 is designed to be varied from V_{SS} to -5V.

C3, C4, R1, and generator ϕ_3 make up the circuit that is used to simulate the input signal. C4 represents the MWPC line capacitance. The capacitance of C3 and the amplitude of ϕ_3 determine the amount of charge deposited on C3. The time required to deposit the charge on C4 is determined by the ramp risetime of ϕ_3 . The resistor, R1, is used to guarantee convergence of the computer program used to simulate the circuit. The time constant, R1C3, is approximately 1 ns.

When no signals are present a bias current will flow through transistors Q5, Q1, Q14 and Q8, Q9, Q15. The bias current establishes the operating point of the common gate pre-amplifier transistors, Q1 and Q9. The bias current is determined by process parameters and VR1 and is given approximately by (assuming no mobility variation with gate voltage):

$$I_{BIAS} = \frac{1}{2} \frac{K_1 K_2}{K_1 + K_2} (V_{R1} - V_{Tn})^2 \quad (2)$$

where,

- K₁ = drive constant of Q1 (Q9)
- K₂ = drive constant of Q14 (Q15)
- V_{R1} = bias control voltage
- V_{Tn} = N-channel threshold voltage

Although there is a strong dependence between bias current and process parameters as evidenced by equation (2) it should be emphasized that the current balance between Q1 and Q9 is important and not the magnitude. The factors that control the selection of the nominal bias current are gm, input resistance, leakage current, and power dissipation.

The leakage current of the common gate transistor and the input protection circuit, which consists of reversed bias diodes, places a lower limit on bias current. The worst case leakage current anticipated is 50 nA. To make the bias current

dominate it was decided that a bias current minimum of 1 μ A would be used. At 1 μ A, Q5 and Q8 can be made minimum size since only a few millivolts will appear across these transistors when they are on. It is desirable to keep these transistors small since they will introduce a switching transient on the sense nodes of the cross coupled pair.

The small signal transconductance and input resistance of the common gate amplifier are given by:

$$g_m = \sqrt{2 C_{ox} \mu \frac{W}{L} I_{BIAS}} \quad (3)$$

and

$$r_{IN} = \frac{1}{g_m} \quad (4)$$

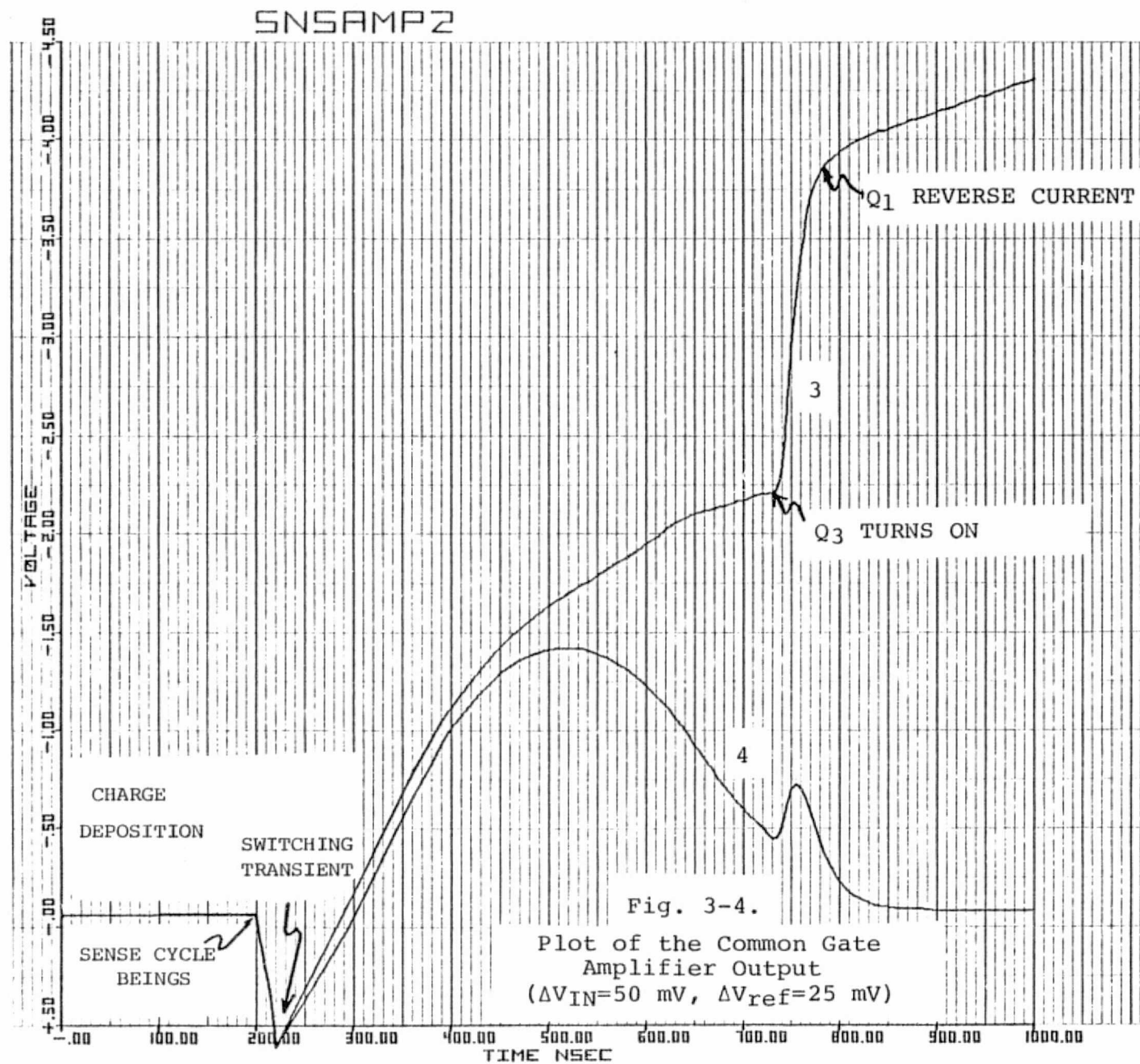
The large signal transconductance is:

$$G_m = g_m + \frac{1}{2} C_{ox} \mu \frac{W}{L} \cdot \Delta V \quad (5)$$

where: ΔV is the magnitude of the input signal, μ = field effect mobility, C_{ox} = oxide capacitance.

It is desirable to have a larger transconductance for the input stage in that it will produce short sense times for small signals. However, a large transconductance will cause an undesirable discharge of the input sense node before the amplifier receives its command to sense. Large signals, in particular, will have fast discharges as seen by equation (5). The design factor having the biggest influence over the discharge of large signals is the W/L ratio of the common gate transistor. A compromise, therefore, had to be reached between the requirement for a large transconductance to shorten the sense time for small signals and the requirement for a small transconductance to reduce charge loss of large signals before sensing.

Figure 3-4 shows the results of a computer simulation of the common gate preamplifier circuit for the case of a small input signal. For this simulation a bias current of about 1 μ A was used. From 0 to 50 ns there is no signal present and, consequently, the nodes are at equilibrium. When the sense amplifier is at equilibrium transistors Q5, Q8, and Q11 are on and Q3 and Q10 are off. From 50 to 150 ns a charge of 0.1 picocoulomb is deposited on C4 which has a value of 2 pf. At 150 ns node 2 has risen by about 50 mV. At this point Q11 turns off and Q10 turns on over a period of 20 ns. 50 ns is allowed for the reference voltage to develop across C2 which is 25 mV. At 200 ns Q5 and Q8 are turned off over a period of 20 ns. This causes a switching transient to appear as evidenced



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by the dip in voltage. This dip is of no consequence providing the switching spike is balanced between nodes 3 and 4. From 220 ns to about 600 ns both nodes 3 and 4 fall in potential due to the bias current which can be viewed as a common mode signal. The rate at which these nodes fall differ due to the differential input signal. At 600 ns a 400 mV differential voltage has developed on nodes 3 and 4. At this point the cross coupled pair, Q6 and Q7, are actively regenerating since their threshold voltage ($V_{TP}=1.0V$) has been crossed by a few hundred millivolts. At 730 ns Q3 is turned on so that a CMOS latch is formed. At about 770 ns the voltage on node 3 is sufficiently lower than that of node 2 to cause a significant amount of current to flow through Q1 in the reverse direction. This causes the charging rate on node 3 to decrease. At 1000 ns nodes 3 and 4 have reached, for practical purposes, CMOS logic levels.

The differential signal appearing across nodes 3 and 4 is fed into an R-S latch which consists of two NOR gates. The latch is designed to offer symmetrical loading to nodes 3 and 4. In the simulation of the sense amplifier the loading of the R-S latch was represented as two capacitors (C5 and C6). When the amplifier is in the idle mode nodes 3 and 4 are at a logic one state which means that the R-S latch is in the "don't care" state. The output of the R-S latch is fed into the shift register.

Figure 3-5 shows the voltage on nodes 3 and 4 as a function of time for the case of no input signal. The reference signal amplitude is 25 mV and the timing of the control signals is the same as in the previous case. Note that at the end of the sense cycle nodes 3 and 4 have the opposite logic states as they did for the case with an input signal present.

Figure 3-6 shows a timing diagram for a large input signal (.75V) and a large reference signal (.42V). Although the sensing cycle is the same as the small signal case the regeneration phase takes place much sooner because of the large signal amplitude. The saturation of the voltage on node 3 prior to ϕ_2 turning on Q3 is due to the voltage on node 3 approaching the voltage on node 2. The voltages that appear on input nodes 2 and 6 are shown in Figure 3-7. Notice that there is some signal loss on node 2 before the reference signal can be applied. This loss can be partially compensated by adjusting the reference signal. The factor that cannot be compensated is the time variation between the input signal and reference signal that will occur from chip to chip. The uncertainty of signal loss is given by:

$$V_{LOSS} \approx \frac{\Delta t}{2C} (2\sqrt{2KI_{BIAS}} + K \Delta V) \Delta V \quad (6)$$

SNSAMP2

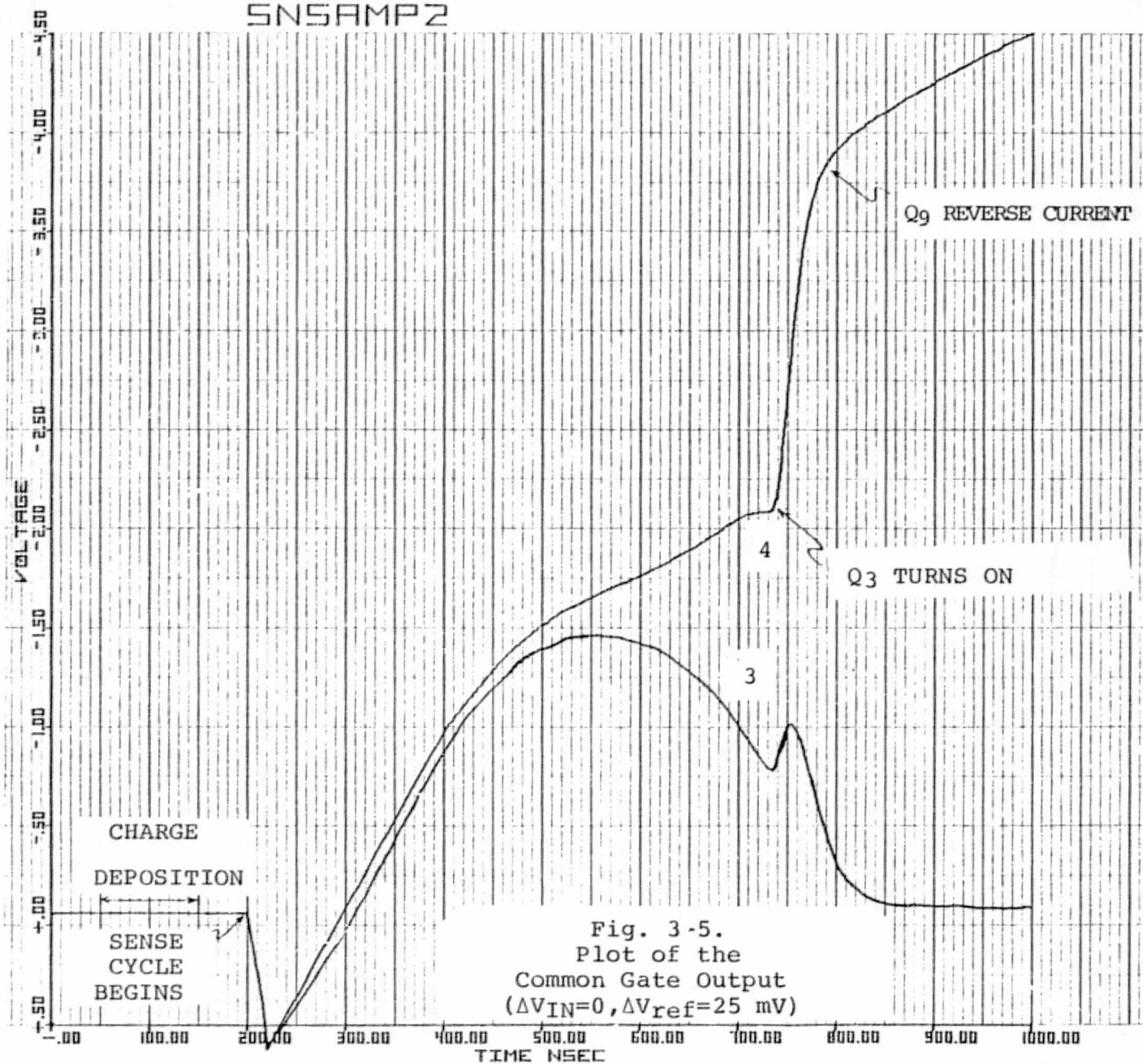
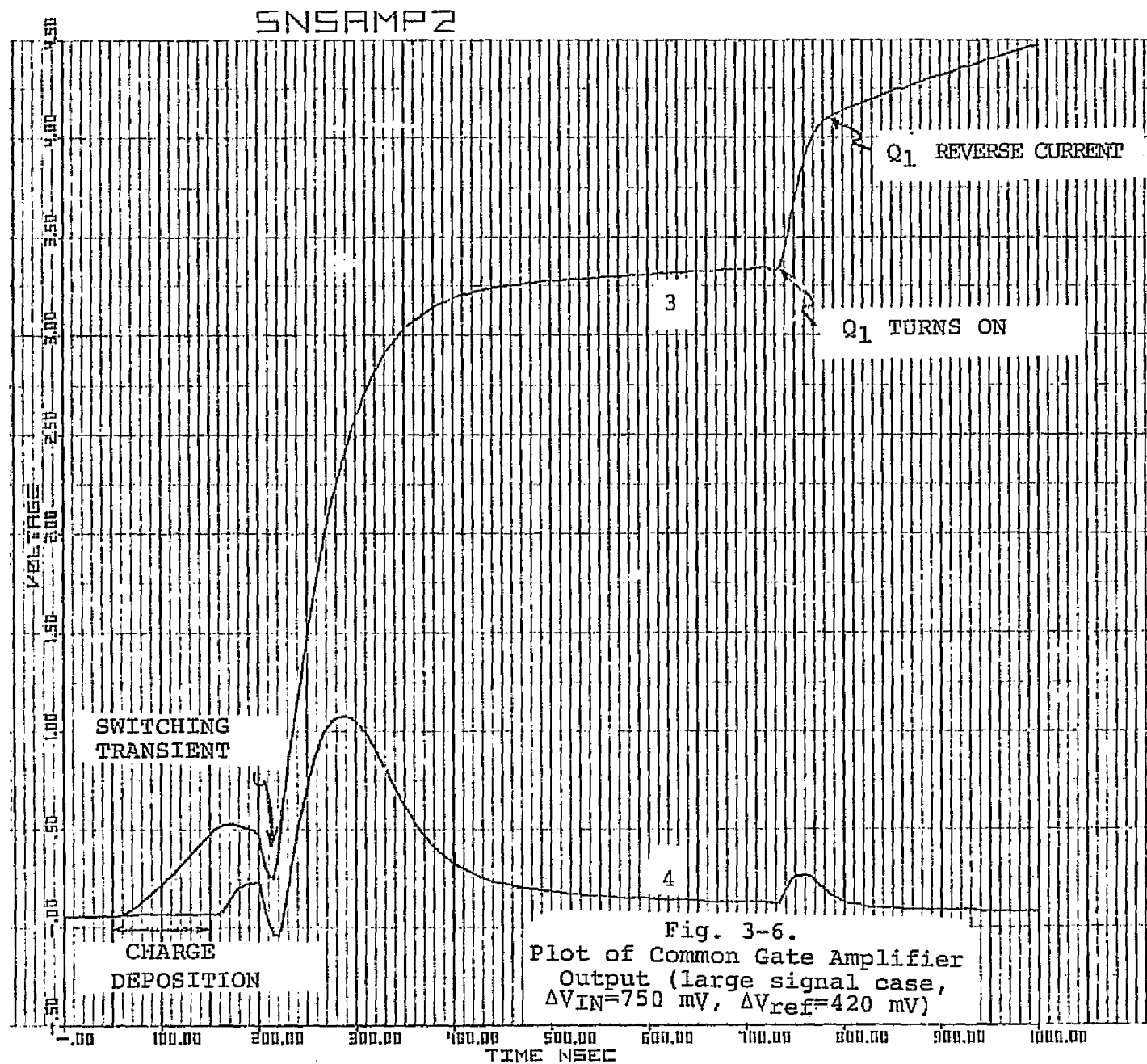
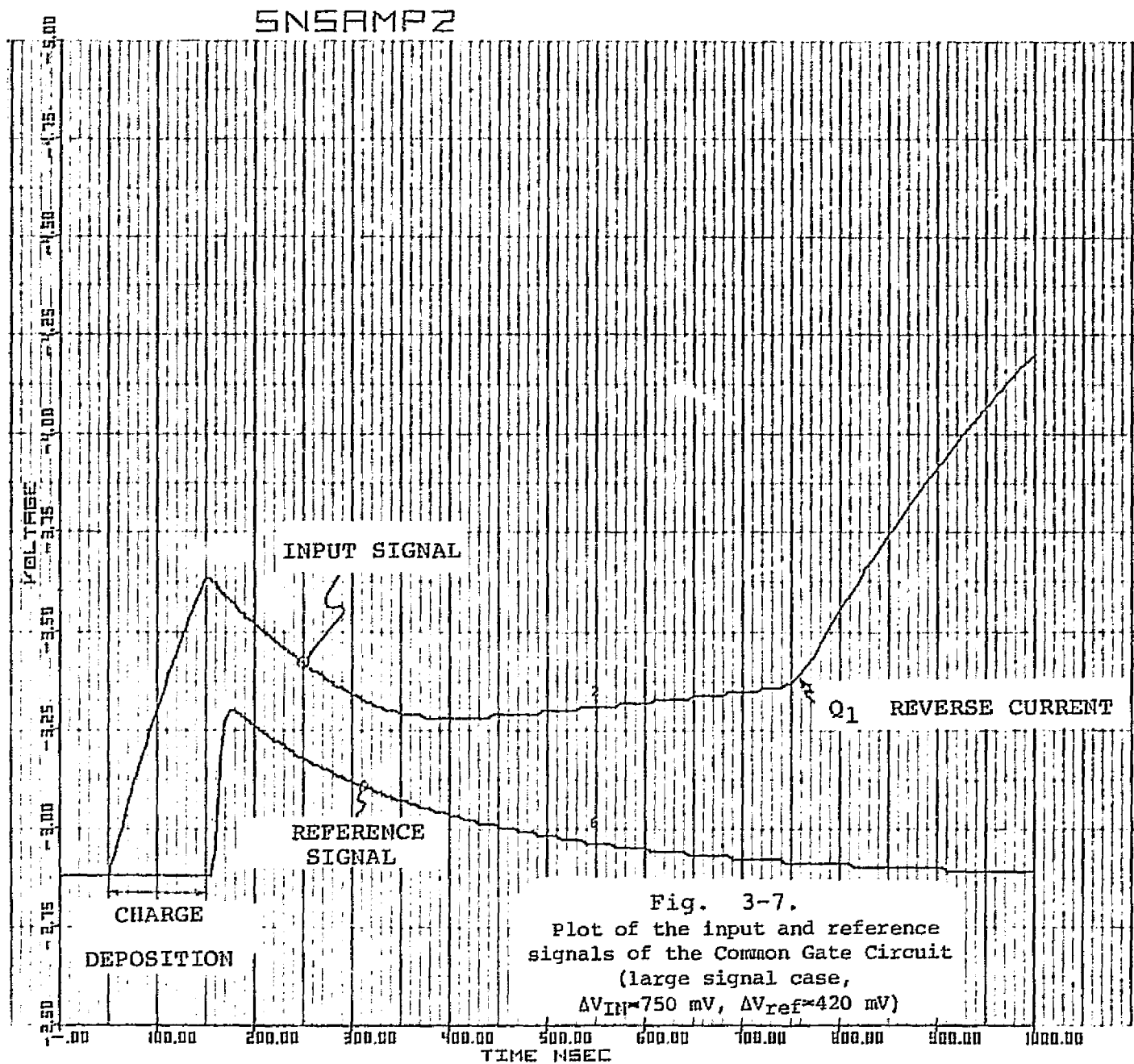


Fig. 3-5.
Plot of the
Common Gate Output
($\Delta V_{IN}=0, \Delta V_{ref}=25 \text{ mV}$)

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where

Δt = worst case time uncertainty between t_{signal} and t_{ref} due to internal delay variations from chip to chip.

C = MWPC source capacitance

K = drive constant for $Q1 = C_{ox} \mu \frac{W}{L}$

ΔV = input signal amplitude

To get an idea of the loss expected for a large signal the following parameters will be assumed:

Δt = 15 nS (This number is based on the assumption that the mean internal room temperature delay (30 nSec) will vary $\pm 50\%$ over temperature and process variations)

C = 2 pF

K = $17 \mu\text{A}/\text{V}^2$

I_{BIAS} = $1 \mu\text{A}$

ΔV = 500 mV

For these parameters, V_{LOSS} is equal to 38 mV. For a small signal amplitude of 50 mV the loss uncertainty is only 2.3 mV. Thus, there will be less signal selectivity for larger signals than for smaller signals due to the uncertainty of the time between the input signal and the reference signal.

The common source amplifier will now be examined. Figure 3-8 is a complete diagram of the sense amplifier along with the circuit used to simulate the input signal and reference signal. Note that the N channel common gate preamplifier has been replaced by a P channel common source preamplifier consisting of Q9 and Q13. Transistors Q7, Q8, Q14 and Q15 make up the bias network while Q16 is used as a V_{DD} return switch. Q1 and Q4 initialize nodes 3 and 4 and are analogous to Q5 and Q8 of Figure 3-3.

The bias requirement for this amplifier is similar to the first amplifier. Because of the input leakage current about $1 \mu\text{A}$ of current is required to flow through Q7, Q8 and Q14, Q15. This bias current is also needed to restore nodes 2 and 6 to their equilibrium value in a reasonable amount of time once the nodes have been perturbed. If $1 \mu\text{A}$ is used to bias the common source stage then the quiescent current for this circuit is two times that of the common gate circuit.

Figure 3-9 shows a simulation of the voltages appearing on nodes 3 and 4 of Figure 3-8. Both the input signal and the reference signal were of the same amplitude as the small signal example of the common gate arrangement. The current used for the bias circuit and the common source transistor was $1 \mu\text{A}$. From 0 to 50 ns no signals are applied to the inputs. Q1, Q4, and Q5 are on and Q6 and Q11 are off. At 50 ns

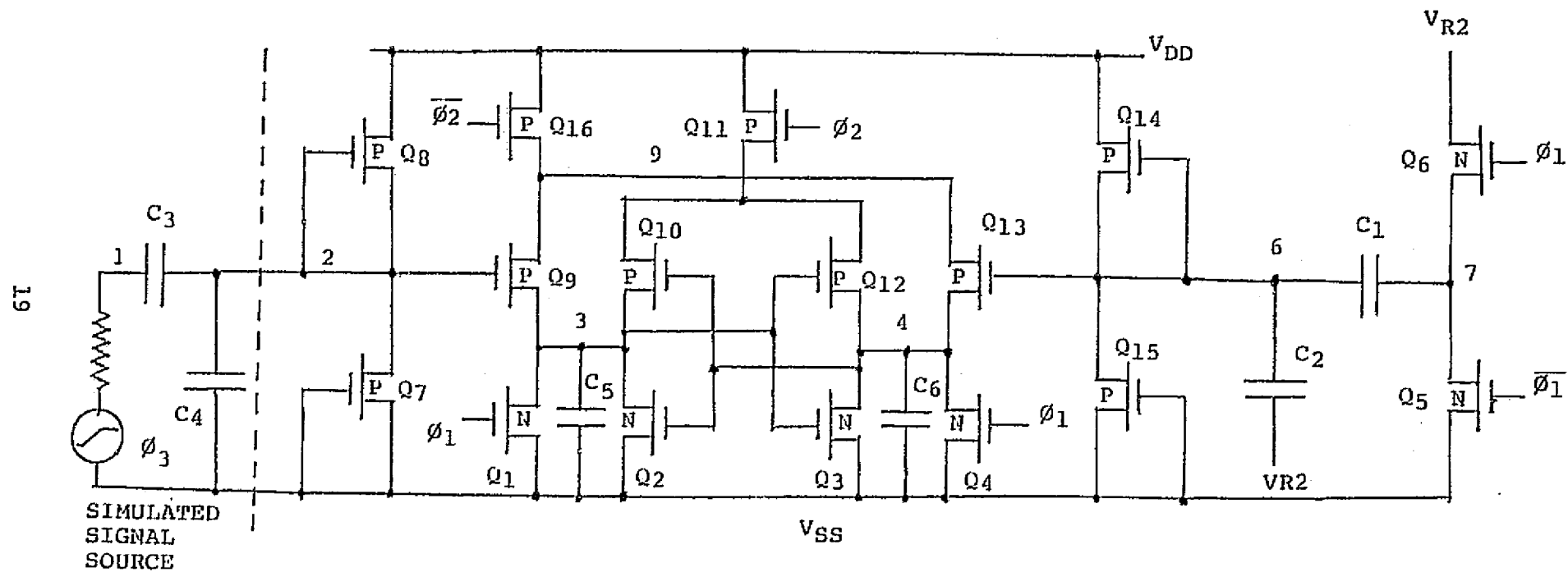


Fig. 3-8. Common Source Sense Amplifier

SENSAMP

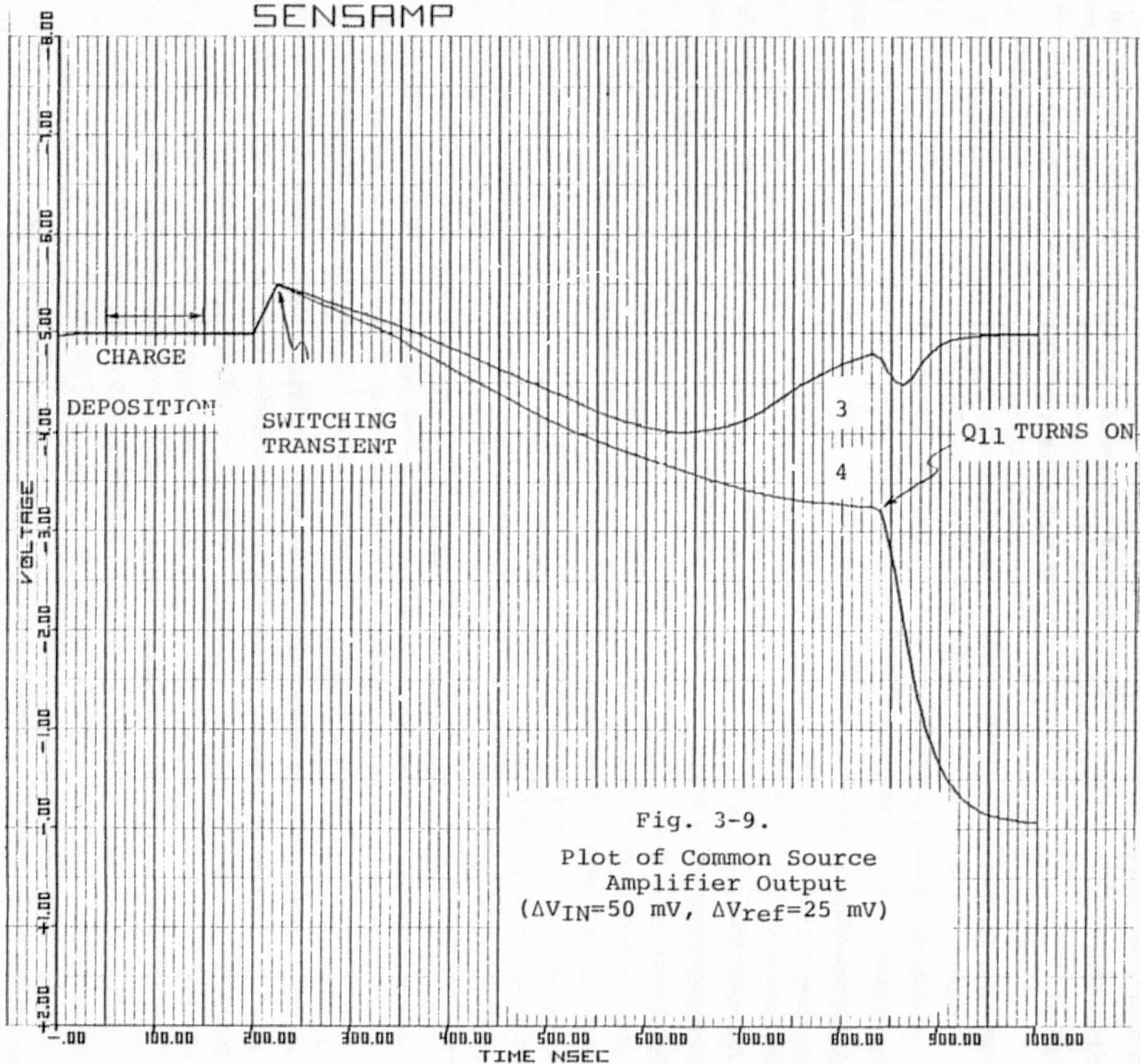


Fig. 3-9.

Plot of Common Source
Amplifier Output
($\Delta V_{IN}=50$ mV, $\Delta V_{ref}=25$ mV)

a charge is deposited on the 2 pf line capacitance over a period of 100 ns. At 150 ns the reference signal is applied by turning off Q5 and turning on Q6 at the same time. The differential signal builds up until regeneration, which takes place at about 600 ns occurs. At 830 ns Q11 is turned on and Q16 is turned off thus allowing the cross coupled latch to reach CMOS logic levels.

The equation controlling the input signal's loss uncertainty for the common source preamplifier is given by:

$$V_{LOSS} \approx \frac{\Delta t}{2C} (K_2(V-V_T)^2 - K_1(V_{DD}-V-V_T)^2), \quad (7)$$

$$V = V_{BIAS} - \Delta V,$$

$$V_{BIAS} = \frac{V_{DD} + V_T \left(\sqrt{\frac{K_2}{K_1}} - 1 \right)}{\left(1 + \sqrt{\frac{K_2}{K_1}} \right)}$$

where

Δt = worst case time uncertainty between t_{signal} and t_{ref}

K_1 = drive constant of Q8

K_2 = drive constant of Q7

C = MWPC source capacitance

ΔV = input signal amplitude

Using the parameters of the first example (i.e. $\Delta t=15$ ns, $C=2$ pf, $I_{BIAS}=1\mu A$, and $\Delta V=500$ mV) and $K_1=6$, $K_2=.34$, and $V_{DD}=5V$ the following value was obtained: $V_{LOSS}=21$ mV. Thus, the common source bias network offers a better V_{LOSS} figure than the common gate network.

An important property of the sense amplifiers that must be examined is the ability of each amplifier to rapidly recover from a spurious input pulse. In the case of the common gate circuit the input is clamped by the input protection diodes to $V_{R1} + 0.7V$ and $-0.7V$. For the common source amplifier the input is clamped to $V_{DD} + 0.7$ and $-0.7V$. If the MWPC source capacitance is charged by a spurious signal to a value outside these limits one of the input diodes will rapidly discharge the source capacitance to one of the limits. The time required for the input node to reach its bias point from one of the limits is determined by the bias network.

Figure 3-10 shows a plot of the input voltage vs. time

RCVYTM

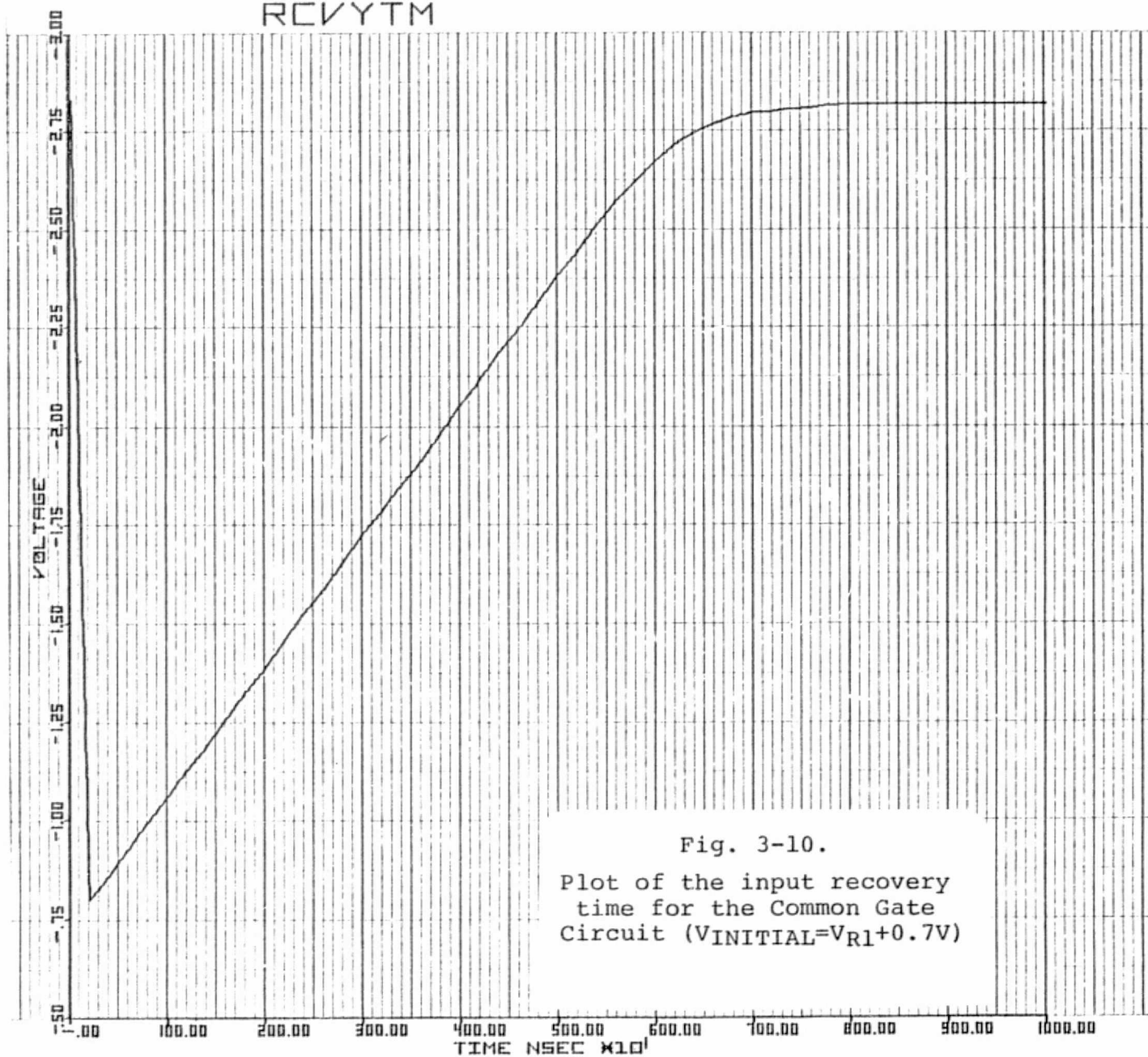


Fig. 3-10.

Plot of the input recovery
time for the Common Gate
Circuit ($V_{INITIAL}=V_{R1}+0.7V$)

for the common gate circuit. At $t=100$ ns the input is perturbed to a voltage corresponding to $V_{R1} + 0.7V$. From this point Q14 (Figure 3-3) discharges the input source capacitance (2 pf) to the bias point. The time required to discharge the source capacitance to within 25 mV of the bias point is 6.8 μS . The table below summarizes the settling times for the common gate circuit and the common source circuit.

SETTLING TIMES*

CIRCUIT ⁺	INITIAL VOLTAGE	SETTLING TIME
Common Gate	$V_{R1} + 0.7V$	6.8 μS
Common Gate	- 0.7	1.8
Common Source	$V_{DD} + 0.7V$	6.6
Common Source	-0.7	3.6

* Time required for the input to come to within 25 mV of its equilibrium value (bias point).

+ Worst case parameters, $C_{SOURCE} = 2$ pf. For typical room temperature settling times, divide values in table by two. For different values of source capacitance, use the scaling factor $C_{SOURCE}/2$ pf.

It was mentioned earlier that the sensitivity of both sense amplifiers will ultimately depend on the degree of balance that can be maintained between the amplifier halves. Figure 3-11 illustrates the three output conditions that will exist statistically about the reference signal. For an input signal below V_{MIN} all sense amplifiers will have a high probability of outputting a logic "0". For an input signal above V_{max} all sense amplifiers will have a high probability of outputting a logic "1". In between V_{min} and V_{max} some amplifiers will output a "1" and others a "0". This offset region is largely influenced by the imbalance within each amplifier. To characterize the magnitude of the offset region the following parameter variations within an amplifier cell will be assumed: $\Delta V_T = \pm 5$ mV, and $\Delta K/K_{AVERAGE} = \pm 5\%$. To simplify the calculation of the offset voltage only the preamplifier section of each amplifier will be considered since this section has the greatest impact on the offset voltage.

Figure 3-12a shows the preamplifier section of the common gate version of the sense amplifier. Using typical values for K_1 , V_{TN1} , K_{14} , and V_{TN19} the average bias current, I_{D1} , can be calculated. Varying the device parameters will cause variations in I_{D1} about the average or typical value. To restore

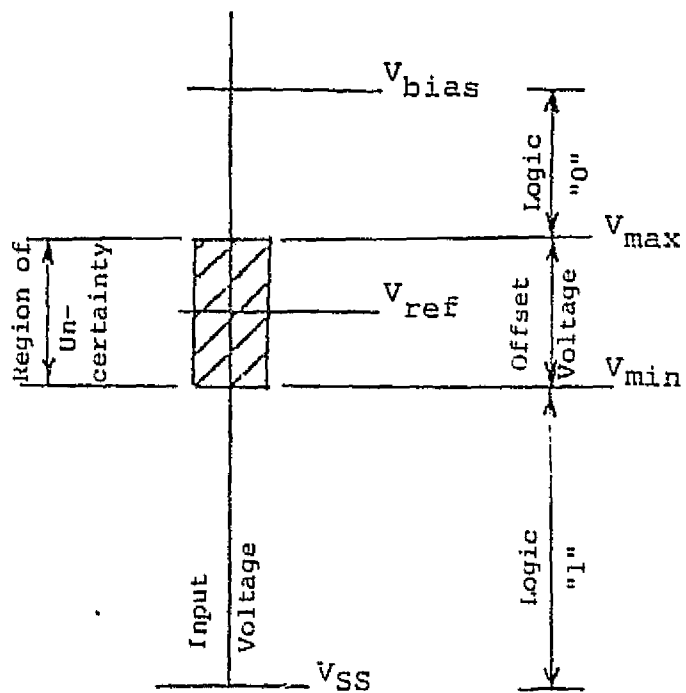


Fig. 3-11 Diagram showing Statistical Output Conditions vs. Input Voltage

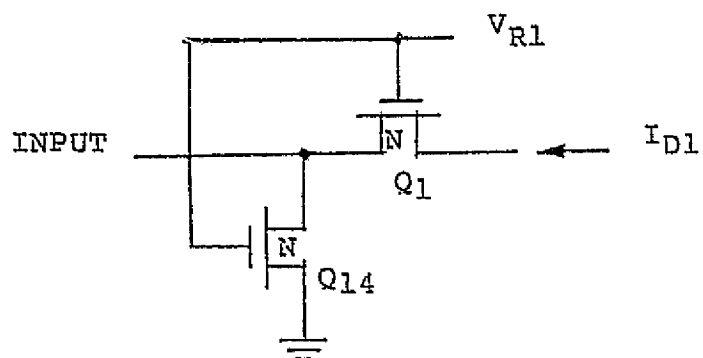


Fig. 3-12a. Common Gate Preamplifier

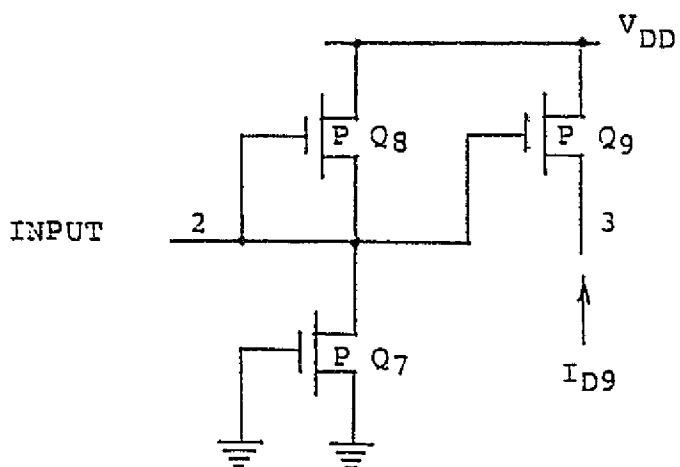


Fig. 3-12b. Common Source Preamplifier

the bias current to its typical value so that there is no bias current differential an offset voltage must be applied to the input (assuming the reference bias current is typical). To find the maximum positive and negative offset voltages for the various combinations of $K_1 \pm 5\%$, $V_{TN1} \pm 5\text{mV}$, $K_{14} \pm 5\%$, and $V_{TN14} \pm 5\text{mV}$, a simple computer program was written. The maximum positive and negative offset voltages were found to be $+0.0107$ and -0.0100 , respectively. This means that an input signal with an amplitude 11 mV above or below the reference voltage will be properly sensed while an input signal with an amplitude within 11 mV of the reference signal will have an increasing probability of being improperly sensed as the input signal approaches the reference signal.

Figure 3-12b shows the preamplifier section of the common source version of the sense amplifier. The maximum offset voltages for this circuit were calculated in a manner similar to that of the common source preamplifier. The maximum positive and negative offset voltages are $+47.7\text{ mV}$ and -46.3 mV , respectively. The reason these numbers are larger than that of the common gate preamplifier is because there is one more transistor and because of bias circuit's sensitivity to imbalance.

3.2.1 Conclusions

Two types of sense amplifiers have been studied - one with a common gate preamplifier, the other with a common source preamplifier. The advantages of the common gate circuit over the common source circuit include lower quiescent current ($1/2$), adjustable bias current (via V_{R1}), and a lower input offset voltage (20 mV as opposed to $\sim 93\text{ mV}$). The advantages of the common source circuit include no V_{R1} supply and a lower V_{LOSS} (21 mV as opposed to 38 mV). Because of the unacceptably high input offset voltage of the common source circuit the common gate circuit is preferred.

3.3 Shift Register

The shift register configuration that was selected for the MWPC project is shown in Figure 3-13. This shift register is an asynchronous, static type register. During serial operation the transmission pair, Q13 and Q14, is turned on while the transmission pair, Q15 and Q16 is turned off. This allows serial data to enter the master section of the register and prevents parallel data from entering. The master section of the register consists of Q5, Q10, Q2, and Q7 with Q3, Q4, Q8, and Q9 forming a feedback circuit used to make the register hold data for static operation. Data is shifted from section to section using complementary clocks, CL and $\overline{\text{CL}}$, to turn transmission pairs or gates such as Q11 and Q12 on and off.

Parallel data is loaded asynchronously into the master section by turning on transistors Q15 and Q16 and turning off transistors Q14 and Q13. This prevents data from entering serially from the D_S input.

Figure 3-14 shows a timing diagram of the master section of the shift register. The diagram is a result of a computer simulation using worst case parameters. Only the master section was simulated since it will have more delay than the slave section due to the parallel/serial control gates (Q13, Q14, Q15 and Q16) present in the master section. To minimize power, minimum size transistors were used. The master section of the shift register will work properly if the delay from the clock edge to the output of the master section is less than 1/2 the clock period (50 ns). As seen from the diagram the delay (34 ns) is less than 1/2 the clock period.

To drive an estimated output load capacitance of 6 pf the last four stages of the shift register were tapered using a geometric progression. A geometric progression as applied to a shift register is the optimum way of tapering the last stages of the shift register for output drive. The progression factor used was 1.3. Since the slave section is faster than that of the master section the progression was started at a slave inverter (the load factor of a minimum size stage coupled into another identical stage is 1 as opposed to 1.3 for the tapered stages). Since the feedback circuits use minimum size transistors the loading caused by these circuits diminishes as the master and slave sections of the tapered stages grow in size. Thus, the increased loading encountered when one stage outputs to a larger stage (by a factor of 1.3) can be offset by the reduced loading of the feedback section. The tapered stages can, therefore, be made to operate at the same maximum

Fig. 3-13. Shift Register

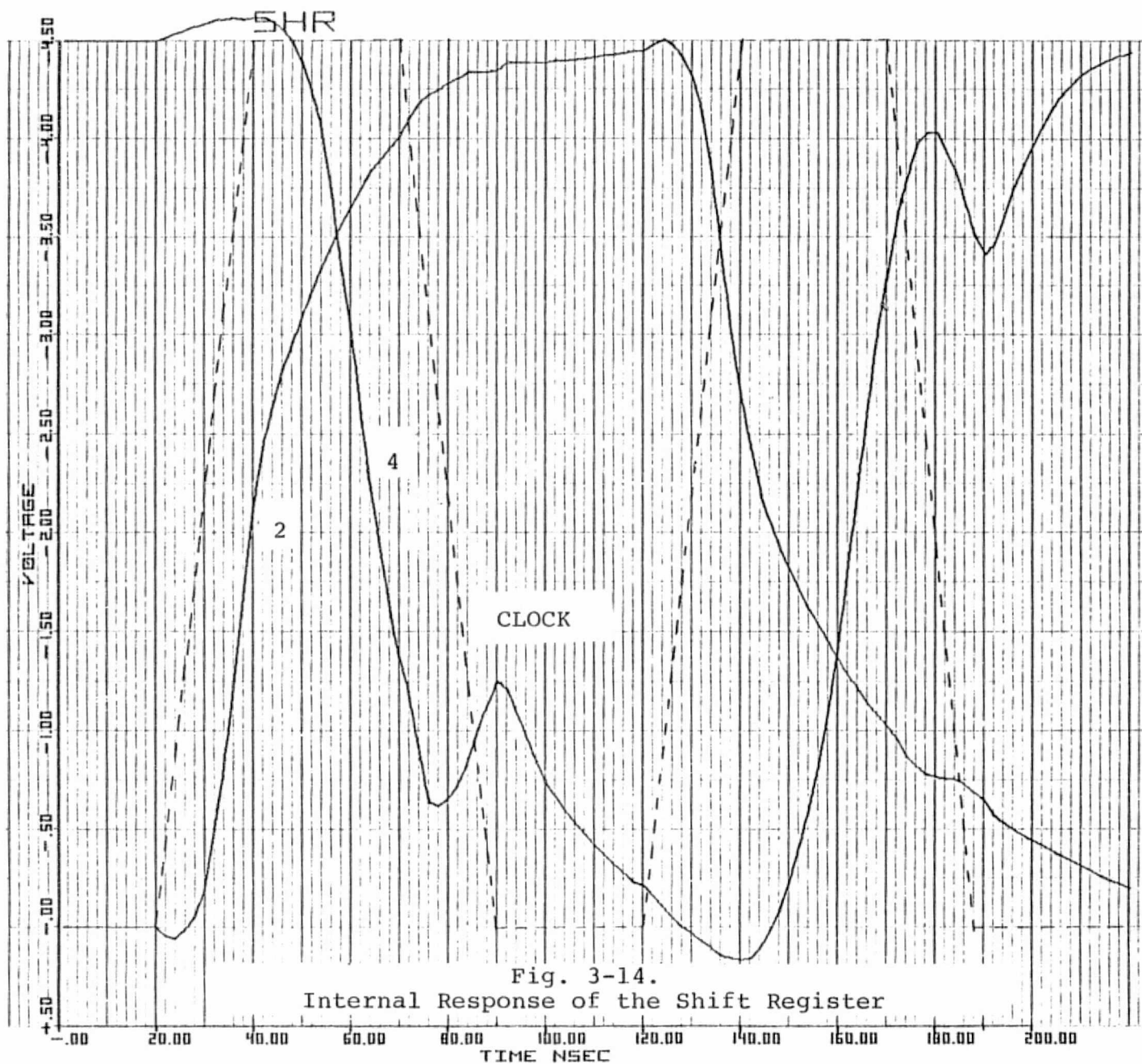


Fig. 3-14.
Internal Response of the Shift Register

frequency as the non-tappered stages.

Figure 3-15 shows the slave section of the output shift register that was simulated. The feedback circuit was omitted since it has a negligible effect on the dynamic operation of this circuit. A non-inverting output buffer consisting of Q3, Q4, Q8 and Q9 was placed between the load capacitance, CL, and the output of the slave section (node 3). Figure 3-16 shows the results of the simulation using worst case parameters. As seen from the diagram the propagation delay from the edge to the output is 48 nS which is less than the 1/2 clock period maximum.

In conclusion it was determined that a shift register can be made to operate at a frequency of 10 MHz under worst case conditions. The shift register will consist of minimum size transistors except for the last four stages which will be tapered according to a geometric progression. The load capacitance for data out was assumed to be 6 pf.

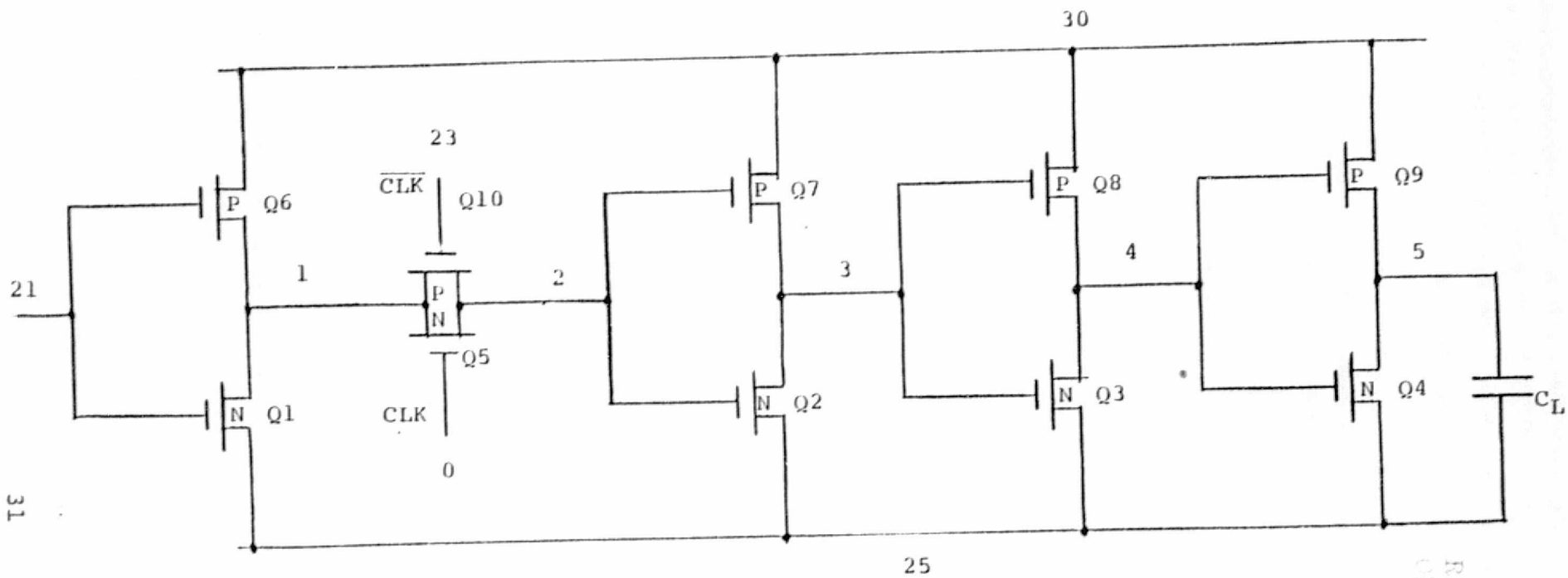


Fig. 3-15. Shift Register Output Stage

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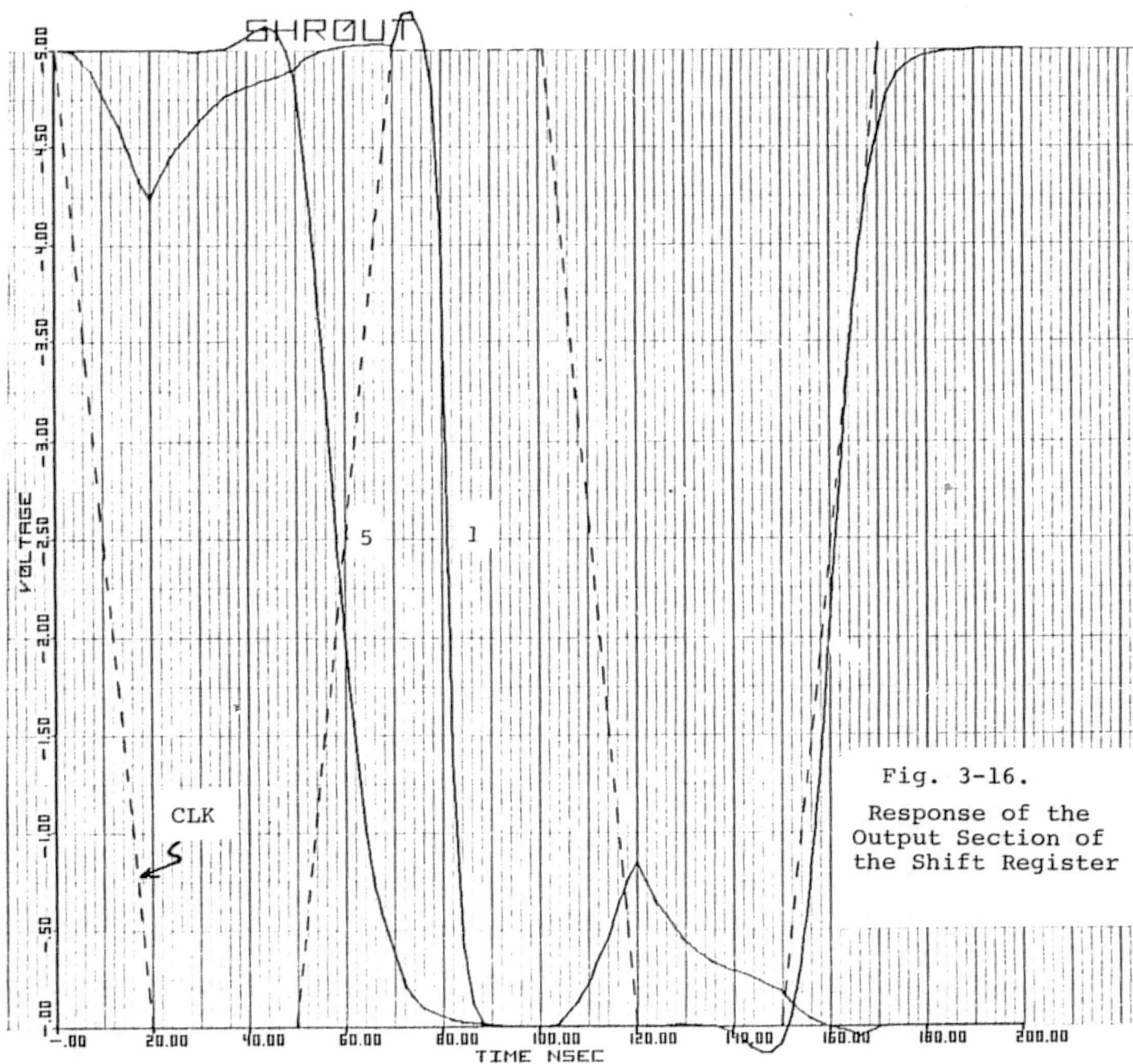


Fig. 3-16.
Response of the
Output Section of
the Shift Register

3.4 Input Protection Circuit

With input capacitances of only a few pf and oxide breakdown voltages of about 60V MOSFET circuits are extremely vulnerable to relatively small amounts of static charge. To significantly reduce the chance of an oxide rupture due to an externally applied static charge an input protection circuit is placed on the chip. This circuit is designed to have a negligible effect on signals within the normal operating range whereas signals outside the normal operating range are severely attenuated.

Figure 3-17 shows a protection circuit commonly used on CMOS/SOS circuits. For input voltages within the limits of $V_{SS}-V_{DIODE}$ and $V_{DD}+V_{DIODE}$ the diodes do not conduct (except for leakage current). The value of the resistor is made as large as possible without making the delay due to the time constant, $R_{IN}C_{IN}$, significant in terms of logic circuit speed. For a signal outside the limits a diode will conduct thus attenuating the input signal. The attenuation factor is given by:

$$A = \frac{R_{ON}}{R_{IN}+R_{ON}}$$

where R_{ON} = the "on" resistance of the input diode. It is therefore desirable to make R_{IN} as large as possible and R_{ON} as small as possible.

The diodes fabricated on SOS, unfortunately, have a large "on" resistance for a given area since they are lateral devices. Figure 3-18 shows a cross section of a gated diode which is commonly used on SOS. The diode is designed so that the surface will accumulate majority carriers when the device is forward biased. The "ON" resistance therefore decreases as the forward voltage increases.

In the case of the sense amplifier there exists a chance that a large voltage (on the order of 1000's of volts) will appear at the input due to a corona discharge between the MWPC sense lines. To aid in the attenuation of this signal a spark gap will be added to the resistor-diode protection circuit. The spark gap consists of a ground line passing within 1.5 mils of the pad. The silox overcoat is omitted between the ground line and pad so that a gaseous discharge can take place across the air gap between the electrodes. The discharge will occur for voltages above about 300V. The spark gap dissipates energy through light emission, sound, and vaporization of the electrode metal. Thus, closer electrode spacing is undesirable because

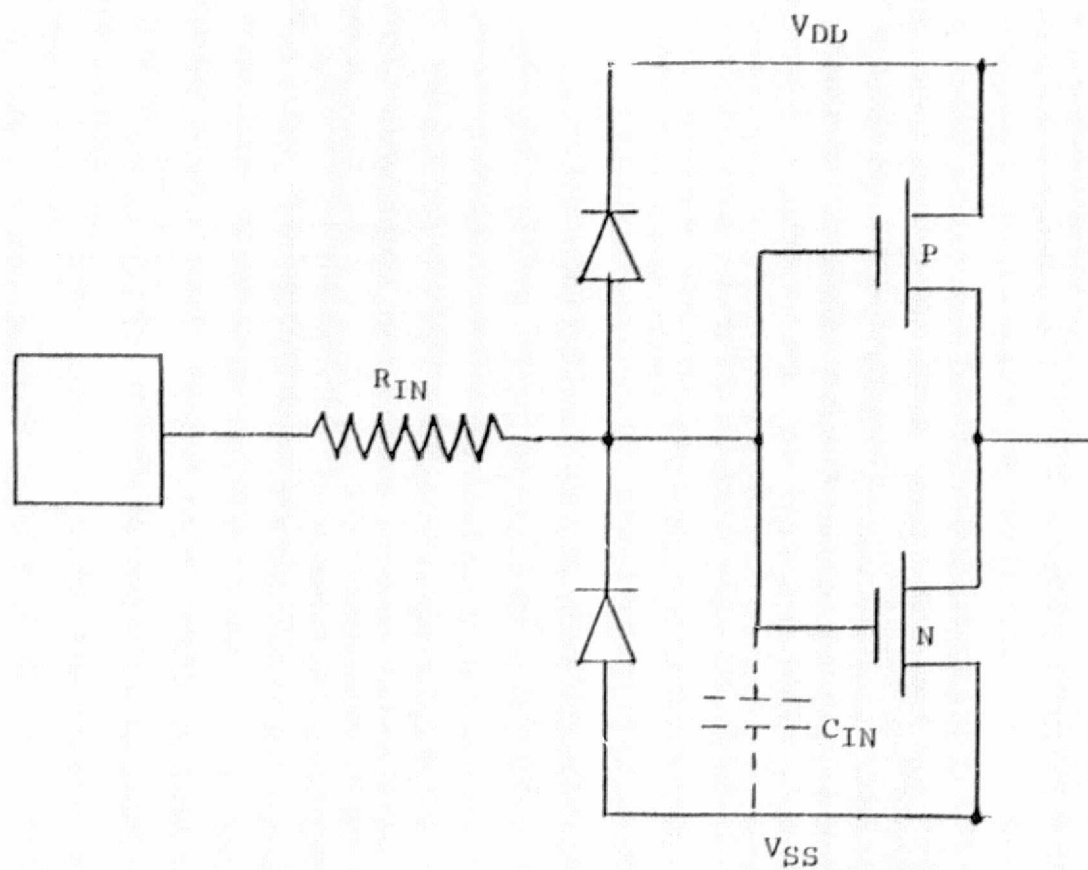


Fig. 3-17. Conventional CMOS Input Protection Circuit

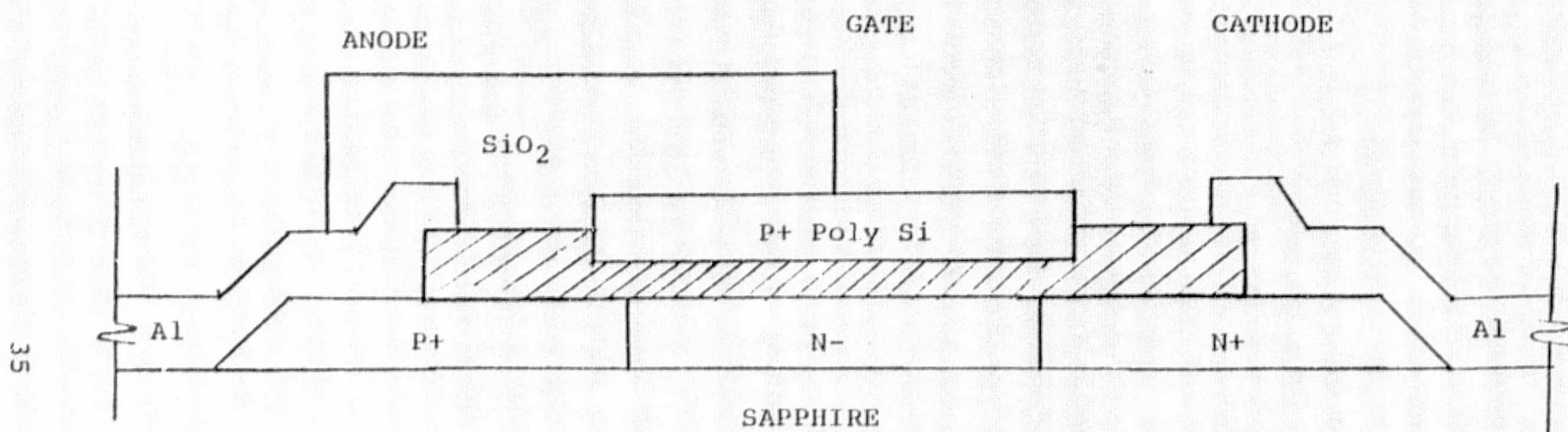


Fig. 3-18. Gated Diode

of the possibility of electrode shorting. The vaporization of the electrode will cause the spark gap to eventually wear out.

The maximum value of input resistance allowed for the sense amplifier is determined by the amount of attenuation the resistor offers to the signals to be sensed. Assuming no more than 1.5% of the signal is to be lost to the input resistor the following equation is used to find the maximum input resistance for the common gate amplifier:

$$R_{IN} \leq \frac{.03}{2\sqrt{2K I_{DO}} + K\Delta V}$$

where

K = drive constant of the common gate transistor

I_{DO} = bias current

ΔV = signal amplitude

For a signal amplitude of 500 mV the maximum value of R_{IN} is 1430Ω. For signal amplitudes less than 500 mV the attenuation will be less than 1.5% (.86% for small signals) for R_{IN}=1430Ω and greater for signals above 500 mV.

To find the attenuation factor for very large input signals the "on" resistance of the diodes must be characterized. The input resistance of the gated diode is largely determined by the resistance of accumulated layer and is given by:

$$R_{ON} = \frac{2V_{GC}(1+\theta(V_{GC}-V_T-V_{DIODE}))}{\mu_{COX} \frac{W}{L} (V_{GC}-V_T-V_{DIODE})^2} \quad (1)$$

where

μ₀ = field effect mobility for small values of surface field intensities,

θ = mobility modulation factor due to the scattering of carriers by the surface,

V_{GC} = gate to cathode voltage,

V_T = V_{FB} + $\frac{qN_{tepi}}{C_{ox}}$ (threshold equation for a thin film transistor)

L = length of the N- region,

W = width of the N- region,

V_{DIODE} = 0.7V

The above equation neglects high level injection effects which lowers the diode resistance below that predicted by equation (1) (equation (1) can be viewed as a worst case estimation of R_{ON}).

The attenuation factor for very large input signals is therefore:

$$A = \frac{R_{ON}}{R_{ON} + R_{IN}} = \frac{2V_{GC}(1 + \theta(V_{GC} - V_T - V_{DIODE}))}{R_{IN} \mu C_{OX} \frac{W}{L}(V_{GC} - V_T - V_O) + 2V_{GC}(1 + \theta(V_{GC} - V_T - V_{DIODE}))^2} \quad (2)$$

For $W/L=50$, $\theta=.03$, $\mu_o=400 \text{ cm}^2/\text{V-sec}$, $V_{GC}=40\text{V}$, $V_T=0.5\text{V}$, and $R_{IN}=1.5\text{K}$ the attenuation factor is 0.10. The magnitude of input voltage needed to produce $V_{GC}=40$ is 400V above $V_{R1}+.07\text{V}$ (or below $V_{SS}-.07$). Thus, for voltages on the order of a few hundred volts the diode-resistor network will be able to provide adequate input protection.

It should be noted that the chances of a large input signal burst destroying any part of the shift register is very remote because of the number of intervening components. Thus, although a sense amplifier may be destroyed by a very large input signal it's shift register won't be. This will allow data from other shift registers to be outputted.

The estimated energy that the input protection circuit can safely absorb is about 10^{-3} pJ . Energies above this value may cause gate-channel or gate-drain/source shorts. One very serious problem is the possibility of a V_{R1} to V_{SS} or a V_{DD} to V_{SS} short. The resistance of a ruptured silicon gate is on the order of $1 \text{ K}\Omega$. Thus, the appearance of a large quiescent current may occur along with a malfunctioning sense amplifier if a high energy input signal is applied.

3.5 Input Buffers

Input buffers provide a variety of useful circuit functions some of which are:

1. Reducing the input capacitance. If an internal node with a large capacitance is to be driven externally an input buffer can be used to reduce the input capacitance. Having a small input capacitance is particularly desirable in the design of an input protection circuit with a high attenuation factor.
2. Improving the rise/fall time of an input signal.
3. Converting the input logic levels to different logic levels.
4. Isolating an internal node with many MOSFET gates connected to it from the package pins. In the MWPC application there are control lines with many MOSFETS connected to these lines. The oxide dielectric strength of an SOS MOSFET is weak at the island edges. Having many MOSFETS connected to an input node enhances the chances of a low oxide breakdown voltage because of the many island edges present. Input buffer transistors can be made edgeless because of their size and, hence, they can greatly reduce the chances of an input having a low gate dielectric strength.
5. Complementing an input signal.

Because of item 4 all control inputs will have input buffers. The two input buffers that will be considered in detail here are the clock and reference control buffers.

Figure 3-19 shows a circuit diagram of the clock buffer used to generate the internal clock signals, CL and $\overline{\text{CL}}$. The circuit has been designed so that the signal delays from the input to CL and $\overline{\text{CL}}$ are equal. Transistors Q5 and Q6 are used as a non-inverting delay element. Figure 3-20 shows the simulation results for the clock buffer circuit. Notice that the CL and $\overline{\text{CL}}$ signals are not skewed.

Figure 3-21 shows the circuit diagram of the level translation circuit required to drive the control transistors of the sense amplifier's reference circuit. The input signal

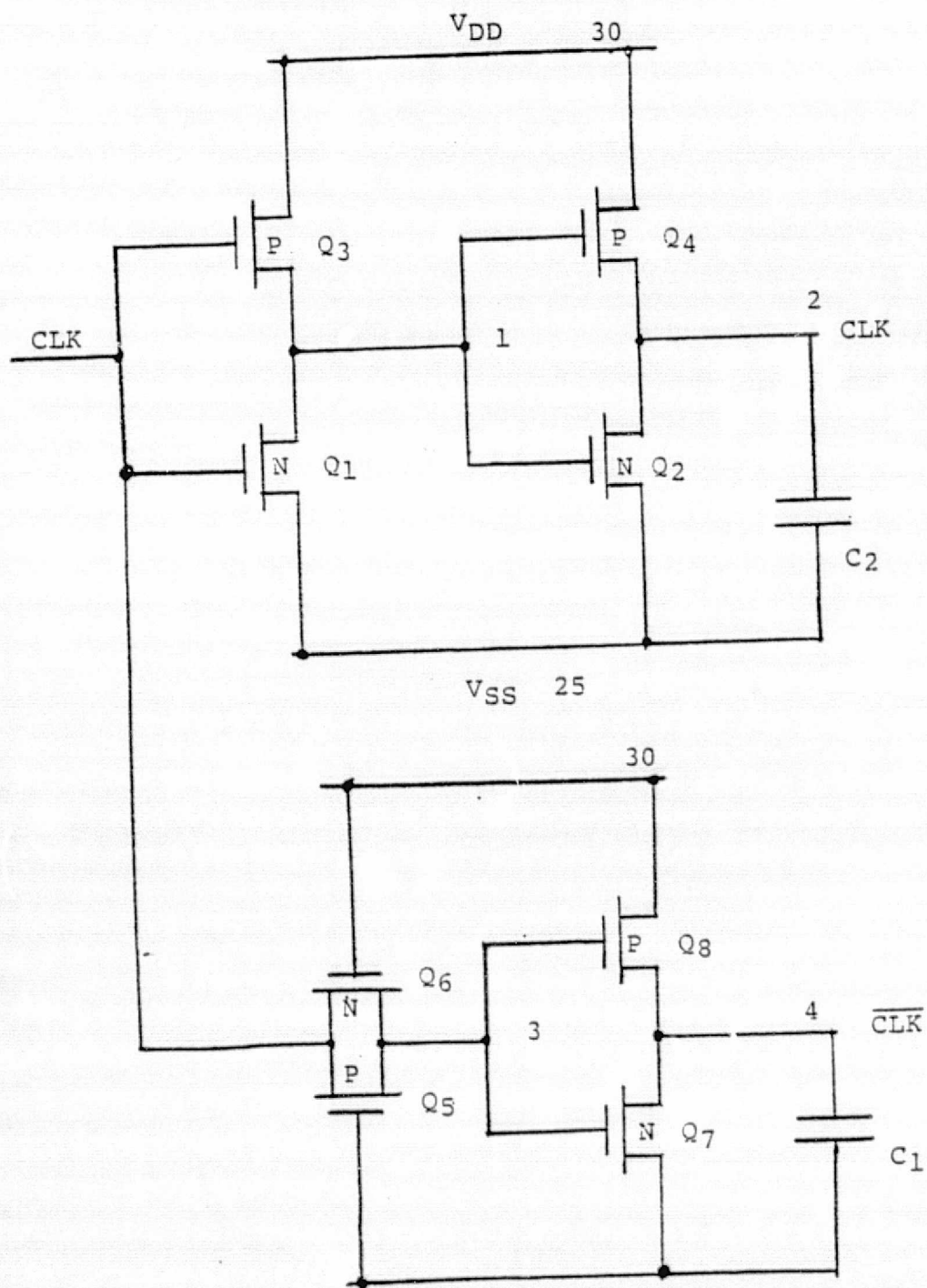
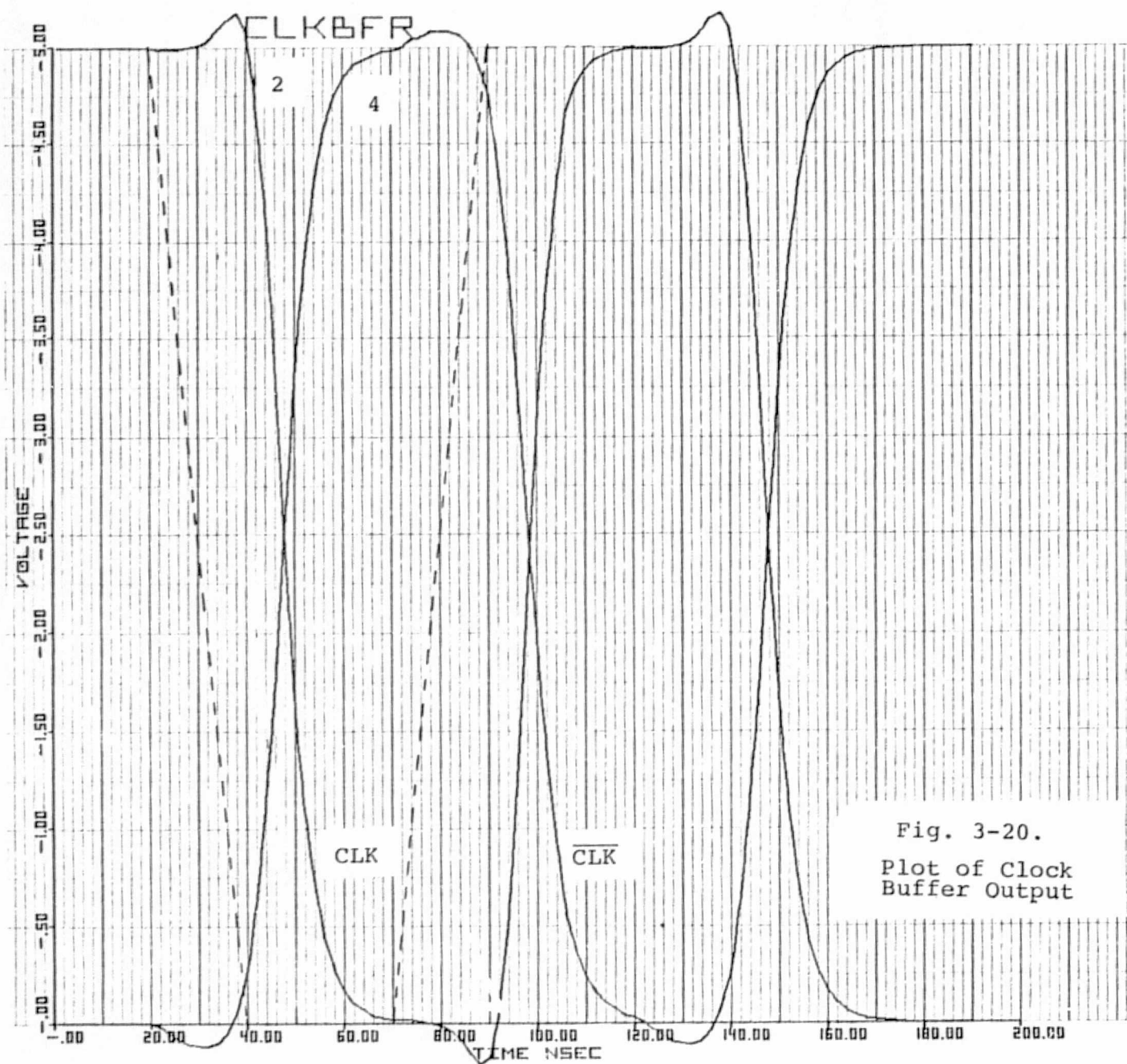


Figure 3-19.
Clock Buffer



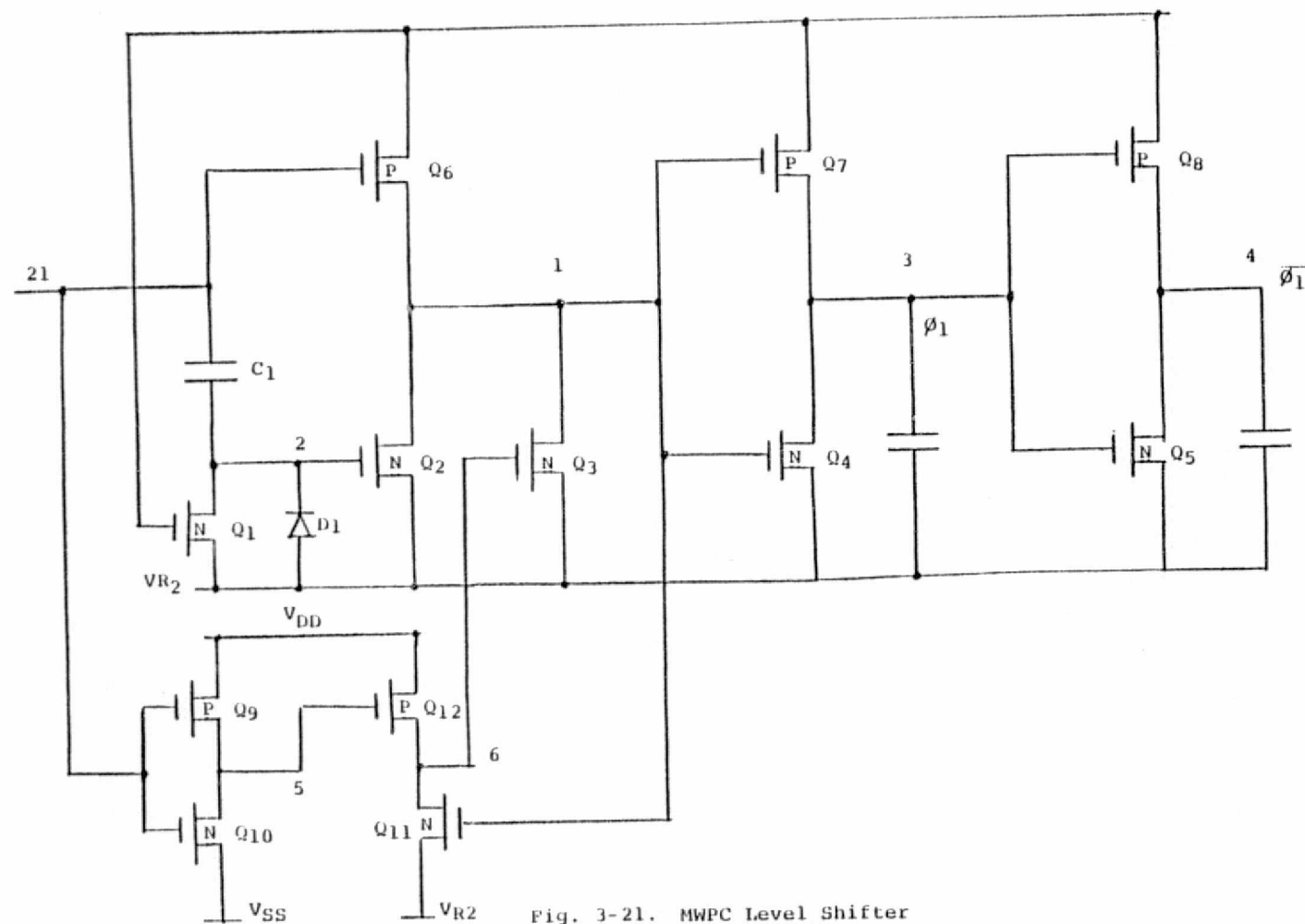
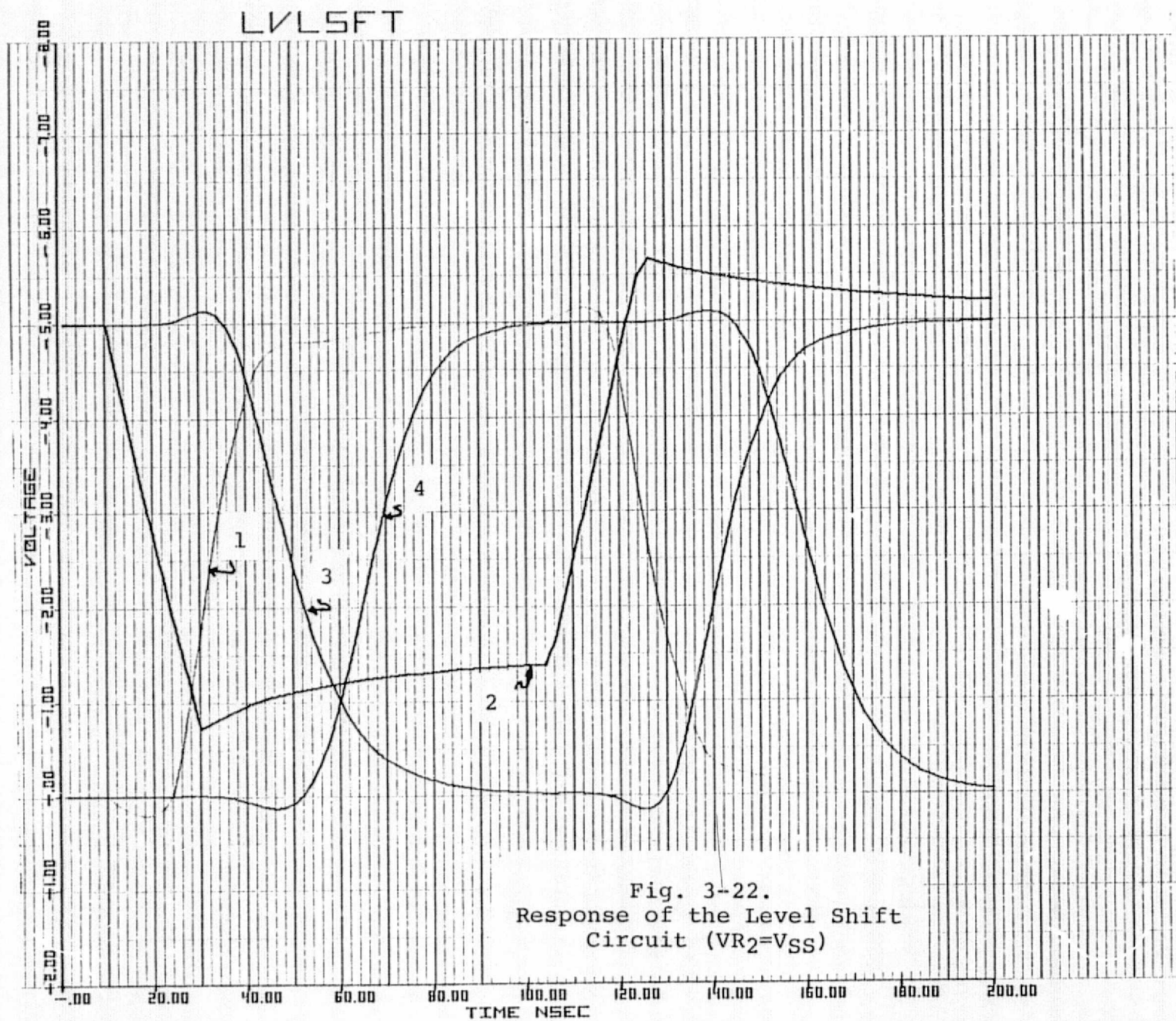


Fig. 3-21. MWPC Level Shifter

has logic levels of V_{SS} (0V) and V_{DD} (5V). The logic levels required by the reference circuit are V_{R2} (0 to -5V) and V_{DD} . The design of this circuit began by first taking a standard inverter connected to the V_{R2} and V_{DD} supplies and considering the effect of the input logic levels of V_{DD} and V_{SS} . With these input levels the P channel device can be turned on and off but not the N channel device because of the V_{SS} - V_{R2} offset which can be greater than the N channel threshold voltage. Since only the signal amplitude is needed and not the D.C. offset the D.C. component of the input signal is removed by a coupling capacitor (C1). A new D.C. level is established by a transistor (Q1) which is used as a high impedance resistor to V_{R2} . Thus, node 2 normally is at V_{R2} which keeps Q2 off. When a V_{SS} to V_{DD} transition appears at the input a V_{R2} to $V_{R2}+V_{DD}$ transition appears (assuming negligible charge splitting occurs) on node 2. Node 2 will eventually discharge to V_{R2} but the rate of discharge is much smaller than the rate of discharge of node 1. Thus, C1, Q1 and Q2 can be viewed as a high speed dynamic pull down circuit for node 1. Diode D1 is used as a fast discharge circuit for C1 when the input goes from V_{DD} to V_{SS} (i.e. if node 2 is at V_{R2} when the V_{DD} to V_{SS} transition occurs node 2 will go negative with respect to V_{R2} and forward bias D1 which will rapidly discharge C1 to within 0.7V of its equilibrium voltage). To retain the logic state on node 1 a slow speed latch circuit consisting of Q3, Q9, Q10, Q11 and Q12 was added. Thus, Q2 rapidly discharges node 1 to V_{R2} while Q3 maintains this voltage. The remainder of the circuit uses conventional CMOS inverters. Figures 3-22 and 3-23 are the plots of the simulation results for $V_{R2}=0V$ and $V_{R2}=-5V$, respectively.

In summary, the circuit of Figure 3-21 has the following characteristics:

- * Highest speed possible for a level translation circuit for a given P and N channel transistor.
- * No quiescent current except leakage.
- * Static operation.



LVLSFT

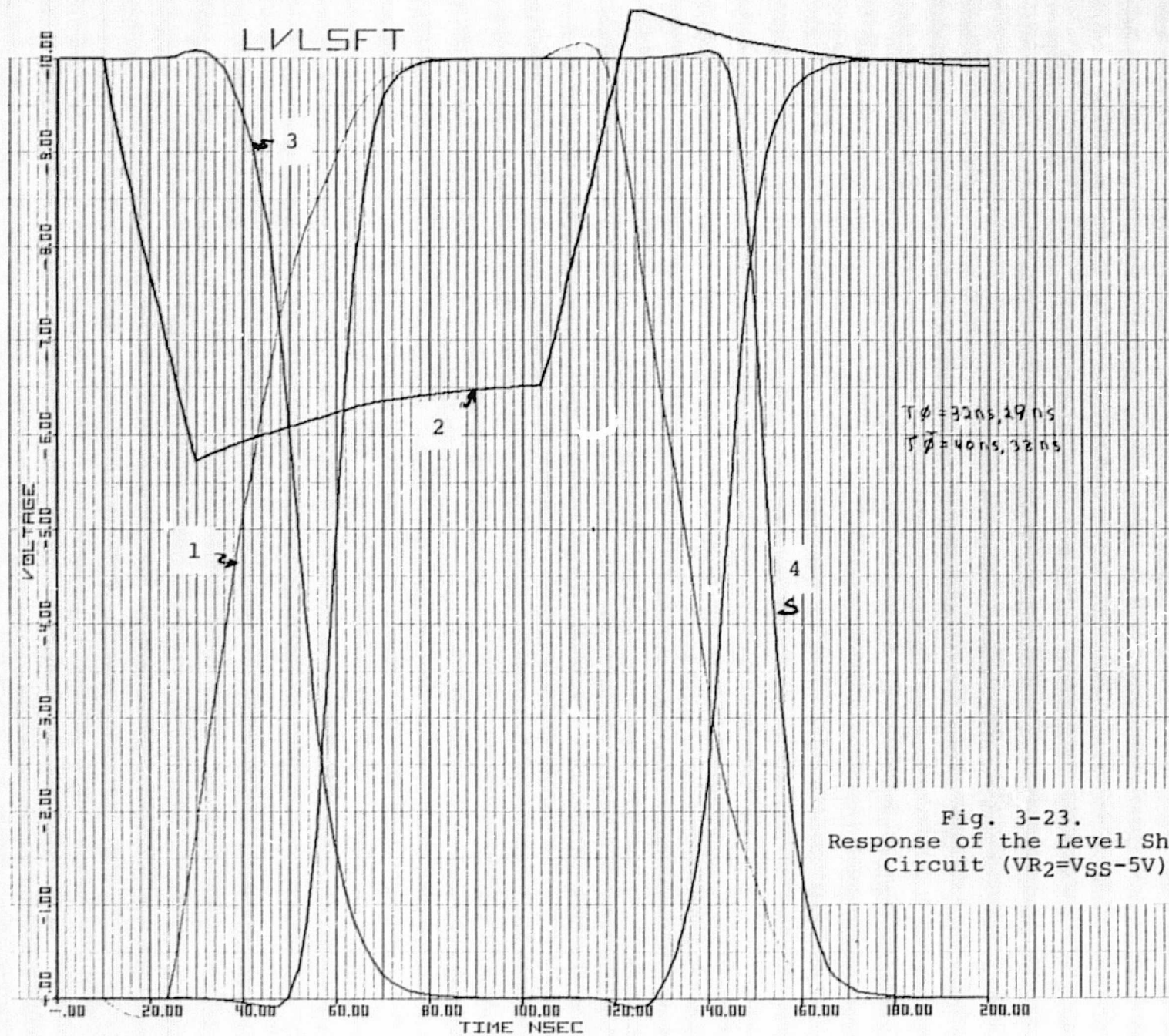


Fig. 3-23.
Response of the Level Shift
Circuit ($V_{R2}=V_{SS}-5V$)

3.6 Circuit Characteristics

POWER

V_{DD}	$-5V \pm 10\%$	V_{R1}	$-3.5V$ typical
V_{SS}	-0	V_{R2}	-0 to $-5V$
V_{DD}	Quiescent power (leakage) = $150\mu W$ (max, 32 bit scheme)		
V_{DD}	Quiescent power (bias) = $320\mu W$ (typical, 32 bit scheme)		
V_{DD}^*	Dynamic power, shift register = 5 mw (32 bit scheme, F=10 MHz continuous)		
V_{DD}	Dynamic power, sense and control circuits = $1200\text{ pJ} \times \text{No. of}$ sense cycles/sec (32 bit scheme)		
V_{R1}	Quiescent power = $0.2\mu W$ max		
V_{R1}	Dynamic power = $45\text{ pJ} \times \text{No. of}$ sense cycles/sec (32 bit scheme, all inputs with large signal present)		
V_{R2}	Quiescent power = $10\mu W$ max ($V_{R1}=-5V$)		
V_{R2}	Dynamic power = $200\text{ pJ} \times \text{No. of}$ sense cycles/sec (32 bit scheme)		
* To save power Clock may be shut off during periods when the shift register is not in use.			

SENSE AMPLIFIER (Common Gate Configuration)

Input impedance = 150 K Ω (typical)	
Input offset = 25 mV (max)	
Bias current = 1 μ A (adjustable via V_{R1})	
Bias voltage (V_{R1}) = 3.5V (typical)	
Reference signal input - - V_{SS} to -5V	
Reference attenuation factor (C_1/C_2)=10:1 (or as specified)	
Input recovery time (to within 25 mV of equilibrium) = 7 μ S max	
Control signals - - See Timing Diagram (Figure 3-24)	

SHIFT REGISTER

Type Asynchronous parallel/serial load; static

Max clock frequency - - 10 MHz

Output load capacitance \leq 6 pf

Clock rise/fall time = 100 nS max

Clock logic levels - - V_{SS} , V_{DD}

Clock edge trigger - - Positive

INPUT PROTECTION CIRCUIT

Type - Resistor, gated diode, spark gap (1.5 mil)

Input leakage - 50 nA max

Estimated max energy dissipation - 10^{-3} joules

CHIP DIMENSIONS

170 X 110 mil (Approximately)

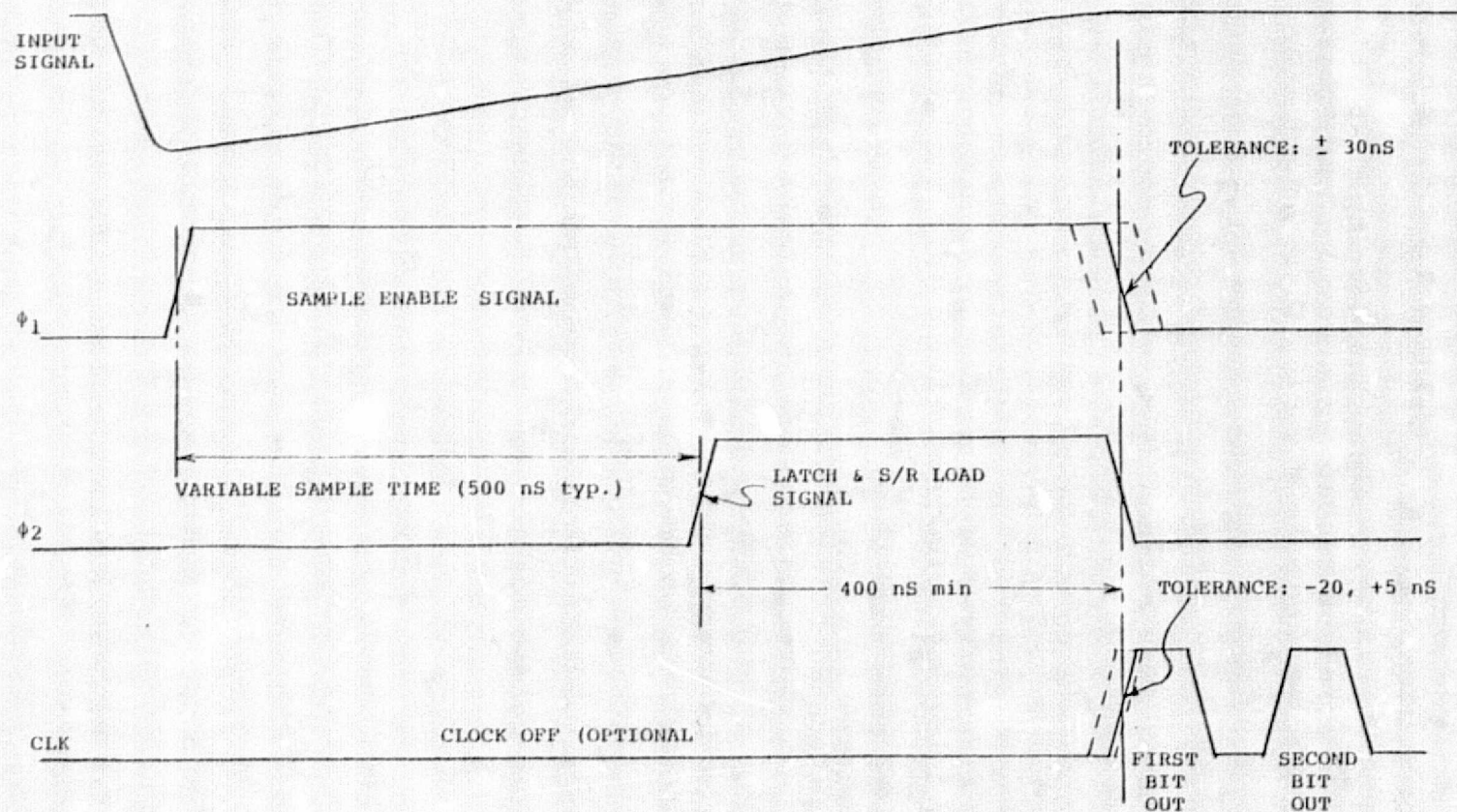


Fig. 3-24. TIMING DIAGRAM

4. FABRICATION AND PACKAGING

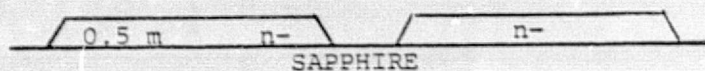
4.1 CMOS/SOS Silicon Gate Processing

Hughes Aircraft Company has developed at it's expense under an Independent Research and Development Program a silicon gate CMOS on sapphire processing technology suitable for use on the MWPC sensing circuits.

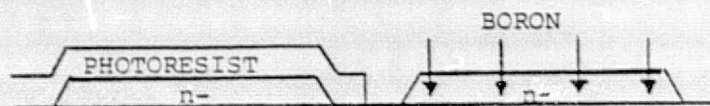
Sapphire wafers with an epitaxial single crystal silicon film 0.5 microns thick (nominal doping $3 \times 10^{13} \text{cm}^{-3}$ n-type) will be used. The silicon films will be doped lightly n-type by ion implantation at the Newport Beach Research Center, where it has been experimentally verified that the doping uniformity achieved by ion implantation is far superior to that which is found in films which are doped during the epitaxial growth. Following the ion implantation step, the wafers are cleaned, a thin layer of oxide is grown, masked (field mask), and etched leaving islands of silicon dioxide where the silicon islands are to be formed. The silicon film not protected by oxide is then completely etched down to the sapphire interface (Figure 4-1a). The silicon dioxide on top of the silicon islands is etched off and a thin layer of oxide regrown on the islands. The wafers are masked (well mask) and implanted with boron where the n-channel transistor will be formed (Figure 4-1b). Next the photoresist is removed, the gate oxide grown, and a layer of boron-doped polycrystalline silicon is deposited and implanted with boron to ensure a low sheet resistance (Figure 4-1c). The polysilicon layer is masked with resist (Si gate mask) and plasma etched (Figure 4-1d). Aluminum is evaporated on the wafers and masked (P+ mask) and etched leaving aluminum over the n-channel transistors. Boron is implanted through the gate oxide to form the self-aligned source and drain regions of the p-channel transistors (Figure 4-1e). The aluminum is stripped, aluminum is re-evaporated, masked (n+ mask) and etched leaving aluminum over the n-channel transistors. Phosphorous is implanted through the gate oxide to form the self-aligned source and drain regions of the p-channel transistors (Figure 4-1f). The aluminum is then stripped off and the field oxide layer is deposited (Figure 4-1g). This is masked and etched to form the contact holes (Figure 4-1h). Aluminum is evaporated on the wafers, then masked and etched, forming the metal interconnects and bonding pads (Figure 4-1i). Finally, a protective overglass is deposited, masked, and etched, opening holes over the bonding pads (Figure 4-1j).

This process (including final passivation) uses eight masking steps. Of these, dimensional control is critical on only four layers (isolation, Si-gate, contacts, metal). The only critical alignments are the silicon gate to island and the contact to silicon gate. This is a significant improvement

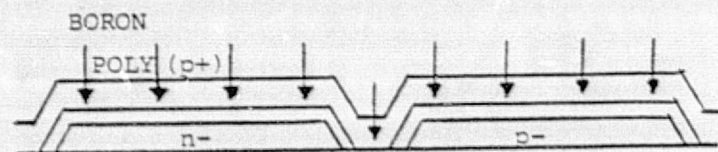
- (a) IMPLANTn-(PHOS)
MASK AND ETCH Si ISLANDS



- (b) MASK WELL
IMPLANTp-(BORON)



- (c) GATE OXIDE
POLYSILICON 0.5μm, p+ DOPED
IMPLANT POLY (BORON)



- (d) MASK AND ETCH POLY
ETCH GATE OXIDE



- (e) EVAPORATE Al
MASK p+
IMPLANT p+ (BORON)

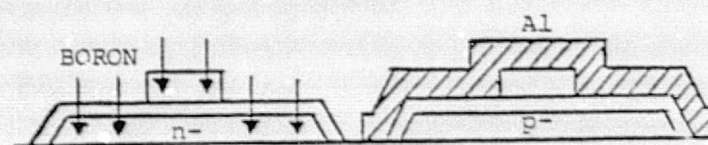
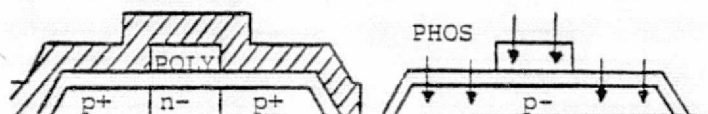


Figure 4-1. CMOS-SOS process sequence

- (f) STRIP Al
EVAPORATE Al
MASK n+
IMPLANT n+ (PHOS)



- (g) STRIP Al
DEPOSIT SiO_2 0.5 μm
DRIVE



- (h) MASK CONTACTS
(POLY CONTACT NOT SHOWN)



- (i) EVAPORATE Al
MASK METAL
(Al-POLY CONTACT NOT SHOWN)



- (j) ALLOY
DEPOSIT OVERGLASS
MASK PAD

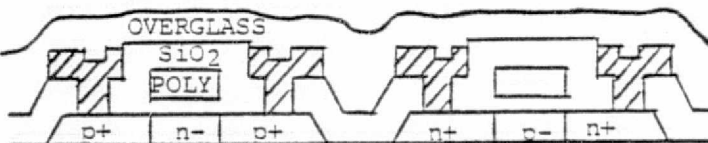


Figure 4-1. Continued

over any bulk silicon CMOS process in common use.

Some of the important features of this process are the following:

- o N⁻ and P⁻ doping are both performed with ion implantation; this provides the most accurate control of the doping levels.
- o N⁺ and P⁺ doping are both performed with ion implantation to minimize lateral diffusion under the polysilicon gate, and thus minimize parasitic capacitance. Both implants are masked by evaporated aluminum, which is subsequently removed. The N⁺ doping is somewhat lighter than the P⁺ so as to avoid serious counter doping of the P⁺ polysilicon gates.
- o Polysilicon is doped during deposition and again by ion implantation (step c) to ensure a low sheet resistance. P-type doping is used rather than N-type because its work-function difference provides more favorable threshold voltages ($V_{TP}=0.5V$, $V_{TN}=+1.1V$).
- o Except for formation of the contact holes, the gate oxide is never etched, ensuring a high gate oxide breakdown voltage as required for adequate input protection.
- o The silox deposition (step g) is performed in such a way that it flows slightly, thus providing excellent step coverage over both the polysilicon and the silicon islands.

4.2 Hybrid Packaging

The preferred packaging technique is to mount the MWPC sensing chip on a thick film hybrid substrate. Ultrasonic wire bonds will interconnect the chip and the substrate.

The thick film substrate package fabrication is based upon multilayer thick film techniques. It differs from conventional multilayer thick film hybrid microcircuits in that this design eliminates the external hybrid package, the hybrid substrate is the package base. The external lead frame can be directly attached to the substrate.

The thick film hybrid substrate can be fabricated by screen printing gold on an unglazed alumina substrate. If

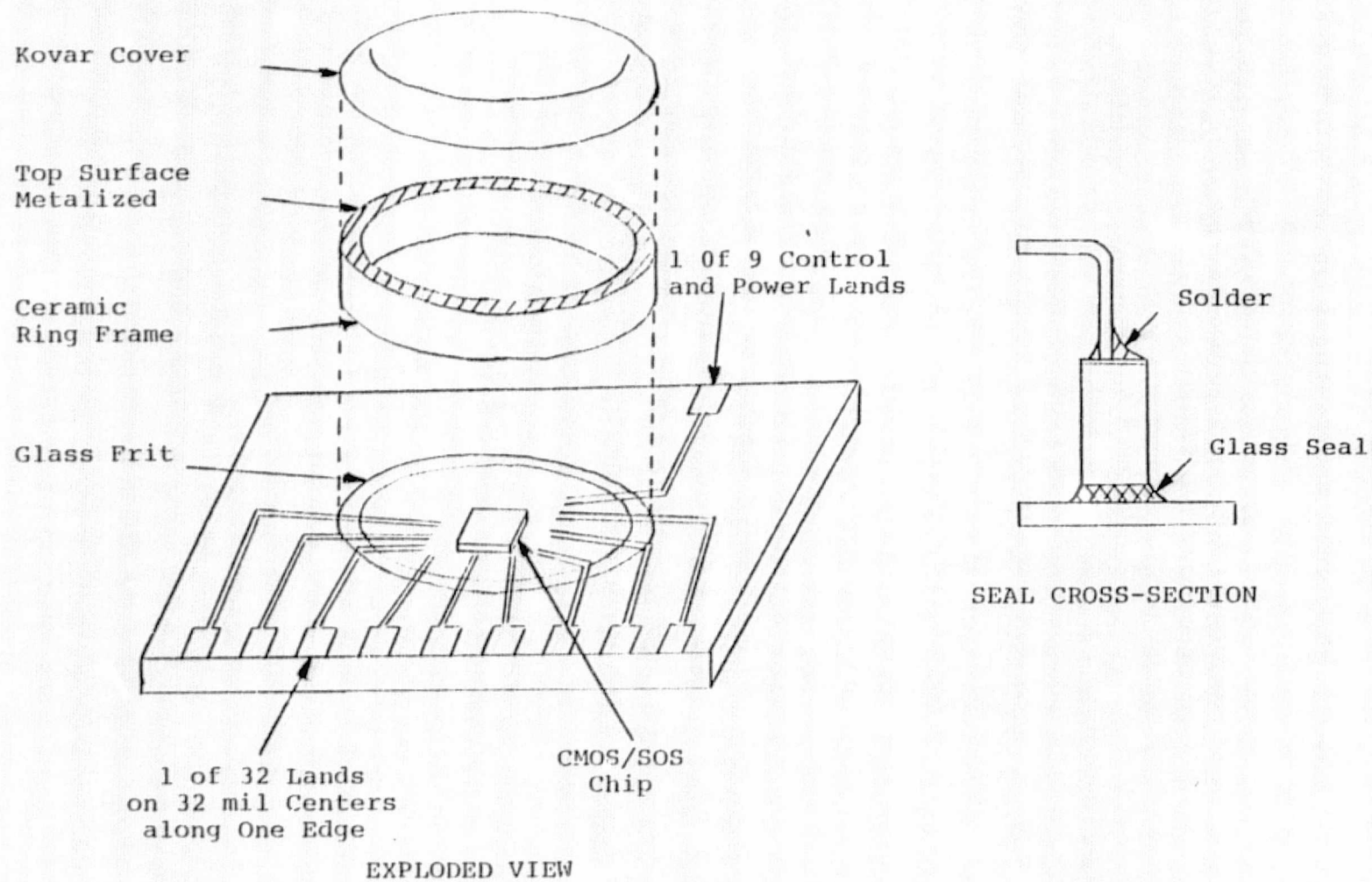


Figure 4-2. Hybrid Package

the gold plated tungsten sensing wires or a lead frame are to be soldered directly to the hybrid substrate, then a platinum-gold film should be screened on over the gold film in the bonding lands. A 60/40 μ A /S_n solder can be screen printed over the Pt/Au film on the bonding lands to ensure that a good solder connection can be made between the tungsten wire and the hybrid substrate. Next a glass frit film can be screened onto the substrate as shown in Figure 4-2. A ceramic ring frame with a gold tin plated Kovar top can then be attached to the substrate by a glass frit seal.

If for some reason it is desirable not to solder the tungsten wires directly to the hybrid substrate, then a lead frame can be welded to the gold lands on the hybrid substrate. These can then be soldered to a P.C. board to which the tungsten sense wires may also be attached.

The CMOS/SOS chip can be mounted on the hybrid substrate either with an organic adhesive or by a gold die attach process developed for sapphire. However the gold die attach process is generally preferred in high reliability applications. Ultrasonic wire bonds can be made between the chip and the hybrid substrate. The assembly should be subject to an internal visual inspection prior to sealing on the Kovar cover. As a minimum the finished hybrid should be screened to Level B of MIL-STD 883A, Method 2004.

5. COST ANALYSIS

5.1 Background

There remain several decisions on the integrated sensing circuits which should have only a minor affect on the overall system performance but may have a significant affect on the overall cost of the Multiwire Proportional Chambers due to their impact on other contractors assembling other portions of the system. In discussing these options, it is assumed that the following decisions have been made and finalized.

5.1.1 Integrated Circuits vs. Discrete Components

The Multiwire Proportional Chamber sensing circuit must be integrated with a single chip accepting multiple signals because the cost, size and power required to implement these functions with discrete devices is prohibitive.

5.1.2 CMOS Selection

The power limitations on the system dictate the use of a low power technology, either Complementary MOS (CMOS) or Integrated Injection Logic (I²L). CMOS was selected for the MWPC application because it consumes significant power only in a dynamic state. I²L, which is essentially a bipolar technology, has a power dissipation which is to first order independent of activity. This will be a distinct advantage in a system which will be active for a few hundred microseconds per event and in standby for a few seconds between events.

5.1.3 CMOS/SOS Selection

The CMOS integrated circuits will be fabricated from silicon-on-sapphire substrates (CMOS/SOS) to permit clocking of the shift register at 10 Megahertz and to minimize the dynamic power. As described previously, the model capacitances in CMOS/SOS are 1/3 to 1/2 those in conventional bulk CMOS. A CMOS/SOS shift register can be operated at 10 Megahertz and 5V but a conventional CMOS shift register will require 10V to operate at 10 Megahertz. Therefore, a conventional bulk CMOS shift register would consume 4 to 6 times more power than the CMOS/SOS shift register in the present application.

5.1.4 Hybrid Selection

The integrated circuit chips will be mounted on hybrid substrates with the lead spacing along one side of the hybrid substrate equal to the wire spacing in the MWPC.

5.2 Cost Trade-Offs

In this section the cost and technical risk of several options will be discussed. Each sub-section will begin with a statement of the feasible options to be considered. Next, the technical advantages and risks will be discussed

5.2.1 Chip Size

Each integrated circuit should be capable of capturing the data from a certain number of sense wires which will be referred to as the number of bits per chip. The three options which were considered are 32 bits per chip, 48 bits per chip and 64 bits per chip.

To more accurately determine the silicon area required for each option, the unit cell containing both the sense amplifier and the minimum size shift register was laid out. This cell, which will occur repeatedly in the chip, is .2mm (8 mils) by 1.13mm (45 mils), including the input pad.

The last five cells in the shift register chain will be somewhat larger than this to provide adequate drive to the next chip. Using this as a guide we estimate the size for a 32 bit chip at 11.16mm² (18,000 mils²), a 48 bit chip at 17.42mm² (27,000 mils²) and a 64 bit chip at 25.81mm² (40,000 mils²). On the 64 bit chip, the size is determined partly by the extended periphery required to accommodate the input/output pads. Increasing the chip area from 11.16mm² (18,000 mils²) for 32 bits to 17.42mm² (27,000 mils²) for 48 bits will reduce the percentage of good die per wafer by 30 to 50% because of the exponential dependence of yield on chip area. This, combined with the reduction in the number of gross die per wafer by 33% will result in an increase in the cost per bit at the wafer level of approximately \$1.40. This will be only partially offset by the lower cost per bit for the hybrid packaging. Therefore, the net increase in cost per bit in going from 32 to 48 bits per chip is estimated to be \$1.10 per bit. Increasing the chip size to 25.81mm² (40,000 mils²) from 11.16mm² (18,000 mils²) is estimated to increase the net cost per bit at the package part level by \$6.45. In addition to far exceeding the design goal of \$4 per bit, the use of a 64 bit chip would increase significantly the program risk. The only significant advantage of incorporating 64 bits on one chip is that a 20% reduction in the dynamic power per bit could be realized because the dynamic power consumed by the output buffer would be averaged over 64 bits instead of 32 bits.

The results of the cost trade-off for different size chips is summarized in Table 5.1.

Table 5.1

Number of bits Per Chip	Estimated Chip Size (mils ²)	Yield Relative to 32 Bits	Increase in Cost per Bit at the Wafer Level	Increase in Cost per Bit at the Package Level
32	18,000	1.0	0	0
48	27,000	.50-.70	\$1.40	\$1.10
64	40,000	.15-.35	\$6.90	\$6.45

5.2.2 Hybrid Size

The sensing circuits must be mounted on a hybrid substrate to achieve the lead spacing required. Present estimates are that the leads will be on 0.8128mm (32 mil) centers. Therefore each 32 sensing wires will add 26.0096mm (1.024 inches) to the length of the hybrid. In the present design the number of leads to each chip is equal to the number of sensing wires handled plus seven leads for power and control signals. If two chips are placed in a single hybrid package, then the number of leads to the hybrid can be reduced by seven. This would require the use of two layers of metalization on the hybrid substrate which would increase the substrate cost. A net cost saving on materials would be achieved since only one substrate and one ring seal would be required. However most of the cost of the hybrid is in the assembly labor which would not be reduced significantly. Furthermore the yield losses experienced in the hybrid assembly operation may be expected to double if two chips per package are used. Therefore unless there are some significant technical or cost advantages in other areas, the use of more than one die per hybrid substrate is not recommended.

5.2.3 Lead Frame Options

Two methods have been considered for an electrical connection between the MWPC sense wires and the appropriate sensing circuits. The wire which has been used on the Spark Gap Chambers is 12.7 to 25.4 micrometer (0.5-1.0 mil) gold plated tungsten wire. 60/40 Au/Sn solder has been used to attach

the wires to a P.C. board. The soldering iron must be kept relatively cool to prevent removal of the gold plating and damage to the P.C. board. One set of connections and the possibility of overheating the P.C. board can be eliminated by soldering the sense wires directly to the hybrid substrate. However, the method in which the sensing wires are strung would have to be modified. Presently a continuous wire is wrapped around the P.C. board frame as shown in Figure 5-1. The wires are initially held to the P.C. board frame by a temporary adhesive. Before removing the anode wires from the frame, the wires are soldered to the P.C. board frame and a second P.C. board is epoxied to the main P.C. board to provide mechanical support for the wire. If the anode wires are to be attached directly to the hybrid substrate, this approach cannot be used since the ring frame and lid on the hybrid would interfere with the wire wrapping operation as shown in Figure 5-1. Instead the wire must be wrapped around the P.C. board frame, permanently attached with another P.C. board for mechanical support, and cut to the desired length before the hybrid is put in place. The individual wires must then be picked up and soldered to the hybrid.

If the above operation can be done in a reasonable manner, then this approach appears to be better for both technical and economic reasons. If it cannot be done, then a lead frame will be attached to the hybrid such that connections can be made to the P.C. board. The additional cost for adding the lead frame is not expected to increase the cost of the delivered part by more than 5%.

5.2.4 Lead Spacing

The plan for the MWPC hybrid at the beginning of the study specified that a lead spacing of 0.635mm (20 mils) would be required. Subsequently the tentative specification was changed to 0.8128mm (32 mils) for reasons not directly related to the hybrid packaging for the sensing circuits. This spacing is within the capabilities of present hybrid technology and will not be a significant factor in the manufacturing cost of the hybrid.

6. CONCLUSIONS

It has been shown that a CMOS on sapphire circuit containing 32 common gate amplifiers and 32 shift register stages can be used to sense 50mV signals (0.1 picocoulombs on 2.0pF or 0.25 picocoulombs on 5.0pF) on 32 parallel inputs, load them into a shift register and shift out the data serially at a 10 Mhz rate. The dynamic power for this circuit should be less than 170 microwatts per bit at 10 Mhz and the standby power should be less than 15 microwatts per bit. Most of the required circuit elements have been designed and simulated, and the results of these simulations show that the proposed design will either approach or exceed the design goals stated in Chapter 2. The wafer processing sequence described in Chapter 4 has been used extensively for fabricating complex LSI circuits with reasonable yields. No new hybrid packaging techniques will be required to permit attachment of the sensing wires on 32 mil centers.

The most cost effective configuration will have 32 sense inputs per chip with each chip packaged on a separate hybrid substrate. If this configuration is acceptable, then the proposed Multiwire Proportion Chamber Integrated Circuits can be produced in quantities of 1000 or more for less than one hundred twenty eight dollars per packaged chip or four dollars per bit.